FE-EE-018 SNS Front-End Systems Technical Note FE3000 October 12, 2000

MEBT Beam Diagnostics Review

P. Cameron, L. Doolittle, M. Kesseleman, S. Lewis, D. Oshatz, J. Power, A. Ratti, and J. Staples

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SNS FE MEBT Beam Diagnostics Review - Oct 12, 2000 AGENDA

Introduction - 8:30 to 9:10 Welcome FE Diagnostics timeline and milestones Commissioning plans and implications for diagnostics	(Rod Keller) (Alex Ratti) (John Staples)	5 min 15 min 20 min
Interfaces - 9:10 to 10:00 MEBT Mechanical layout EPICS interface, ground rules, software compatibility	(Daryl Oshatz) (Steve Lewis)	20 min 30 min
Float		15 min
BPPMs - 10:15 to 11:15 Electromagnetic design and measurements Position/phase electronics & PCI interface Discussion	(Larry Doolittle) (John Power)	20 min 30 min 10 min
BCMs - 11:15 to 12:00 Electromagnetic design and measurements Electronics processing Discussion	(Larry Doolittle) (Marty Kesselman)	15 min 15 min 15 min
Lunch - 12:00 to 1:00		
Profile measurements - 1:00 to 2:20 Envelope and accessibility Wire scanners/heating/actuator Discussion	(Daryl Oshatz) (Pete Cameron)	25 min 30 min 25 min
Float		10 min
Wrap-up - 2:30 to 3:30 Project Management needs Reviewer Discussion Closing Remarks	(Rod Keller) (Tom Shea)	10 min 40 min

Project Timeline & Milestones

~ Alex Ratti

Commissioning Plans & Implications for Diagnostics

~John Staples

MEBT Mechanical Layout

~Daryl Oshatz

EPICS Interface, Ground Rules, & Software Compatability

~Steve Lewis

BPM Electromagnetic Design & Measurements

~Larry Doolittle

BPM Positron/Phase Electronics & PCI Interface

~John Power

BCM Electromagnetic Design & Measurements

~Larry Doolittle

BCM Electronics Processing

~Martin Kesselman

Profile Monitors Envelope & Accessibility

~Daryl Oshatz

Wire Scanners/Heating/Actuator ~Pete Cameron





FE Scope, Status, Schedule and Interfaces

Alessandro Ratti





- Need/motivation for this review
- Current status
- Current FE schedule and major milestones
- Main interface points



Motivation and Description



- Review the status of the MEBT beam diagnostics package
 - Scope and technical design
 - Project needs
 - Project interface points
- Define schedule, deliverables, interface points and responsibilities
- Requirement by SNS project office



Scope of MEBT Diagnostics



- 7 Beam Position Monitors
 - Position and phase reference
- 2 Beam Current Monitors
 - Rise/fall time and total charge
- 5 Profile monitors
- Emittance Measurement Device





- Level of completion
 - In final stage:
 - BPM
 - BCM
 - At a conceptual level:
 - Profile monitors
 - At feasibility stage:
 - Emittance scanners



Status of hardware

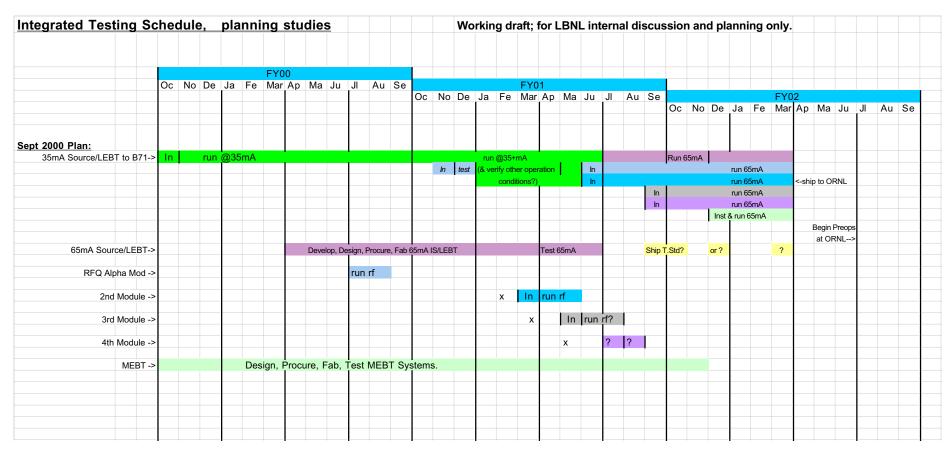


- Have BCMs
 - Some measurements available
- Have BPMs
 - Some measurements available
- Need electronics for BCMs and BPMs
- Emittance scanner:
 - Mechanical feasibility study underway
 - Have conceptual design 64 channel pick-up electronics



FE Schedule





Berkeley Lab — Accelerator and Fusion Research Division — Ion Beam Technology Program

A. Ratti: MEBT Dia Rev. 001012



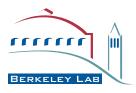
FE Schedule - Interface Points

- Jul 1, 2001 Start rafts assembly
 - Need ALL Vacuum components and NO external hardware
 - Start bench test of components
- Jul 1, 2001 Begin runs with 2+ RFQ modules
 - Can do beam tests of diagnostics
 - BPM, BCM, Wire Scanner
- Dec 1, 2001 Install MEBT in the beamline
- Jan Mar, 2002 MEBT commissioning at LBL





- At LBNL
 - BCM Mechanical
 - BPM Mechanical
- Collaborating labs
 - Profile Monitors (BNL)
 - Electronics
 - BPM needed by Jul 01 (LANL/LBNL)
 - BCM needed by Jul 01 (BNL)





- LBNL defines mechanical envelope
 - i.e. Profile Monitors
- Collaborating labs define/provide signals
- EPICS prepared to accept/process signals
- Provision for interface with RTDL at ORNL
- Other ORNL interface points
 - PPS, TPS systems



FES Commissioning

John Staples, LBNL

12 October 2000

Overview



- FES Tuning
- Beam Parameter Range
- Diagnostic Plate
- Warmup
- Training and Safety
- Issues beyond FES

FES Tuning



• Knobs:

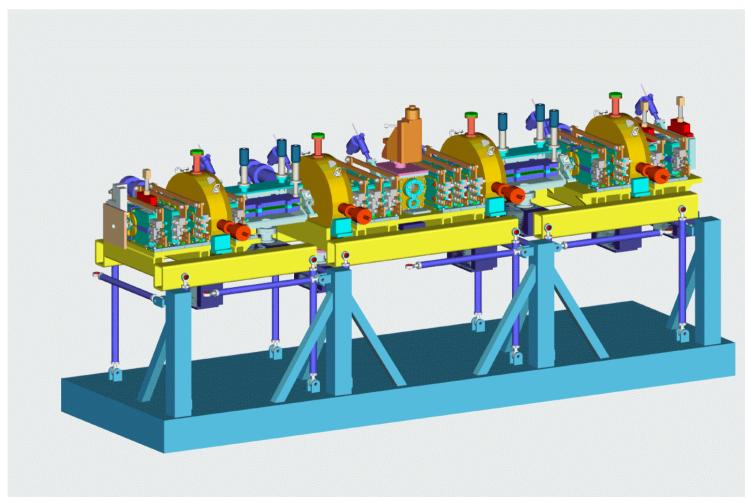
- 11 quad (central 6 quads in 3 families
- 8 rebuncher (4 amplitude, 4 phase)
- 12 steering (6 x, 6 y steerers)
- Chopper target position

Diagnostics

- 5 x, 5 y profile (wires, non-intercepting later)
- 6 x, 6 y centroid from 6 BPMs
- 6 phase monitors from same 6 BPMs
- 2 toroids
- Emittance device (very low power)

MEBT Layout



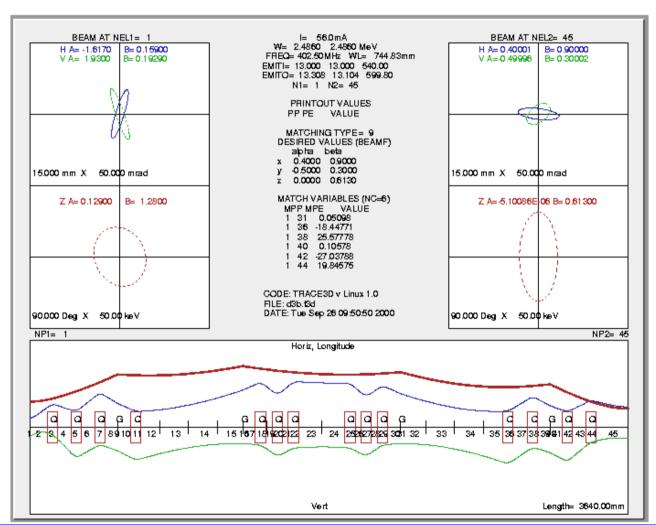


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MEBT Beam Envelope



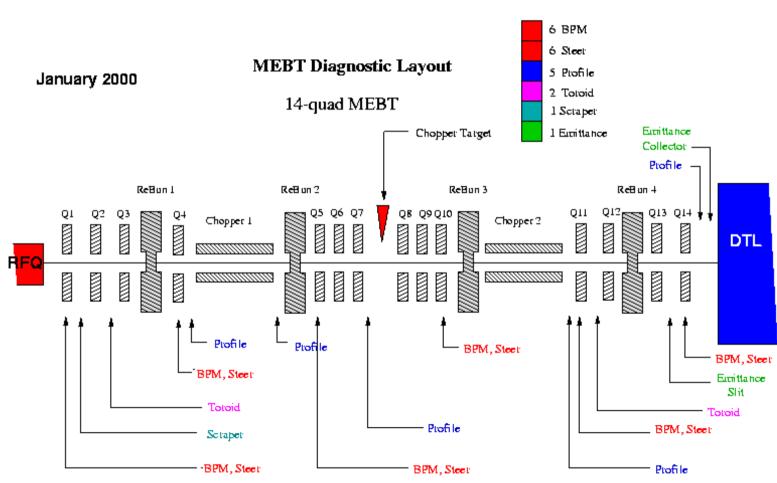


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MEBT Diagnostics





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Ion Beam Technology Program

FES Tuning 2



- Diagnostics give slightly overdetermined set
- RFQ characteristics assumed known
 - fairly independent of ion source emittance
- Redundancy:
 - Quads: mag measurements + beam-based
 - Cavities: r.f. probes and TOF
- MEBT chopper power supply:
 - run at low or d.c. to set $M_{16}=M_{26}=0$

Beam Parameter Range



- Full 2 MW operation
- Enhanced, for 2-ring operation
 - implications of supercycle interaction
- Reduced Specs
 - single-turn for ring studies
 - low current
 - full current, low duty-factor
 - other special tuning/operation modes

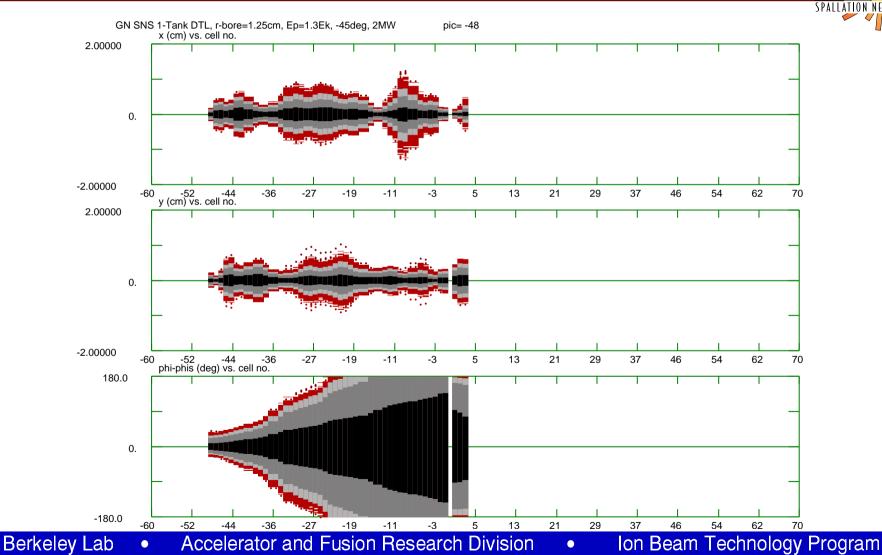
Rebuncher Cavity Tuning



- 4 Cavities, tune amplitude and phase of each
- Use TOF technique with BPMs
- Observe 805 MHz beam component
- Beam debunches fast: make sure that enough survives to do a TOF measurement
- Turn on rebuncher in sequence
- No pulse shape monitors in MEBT

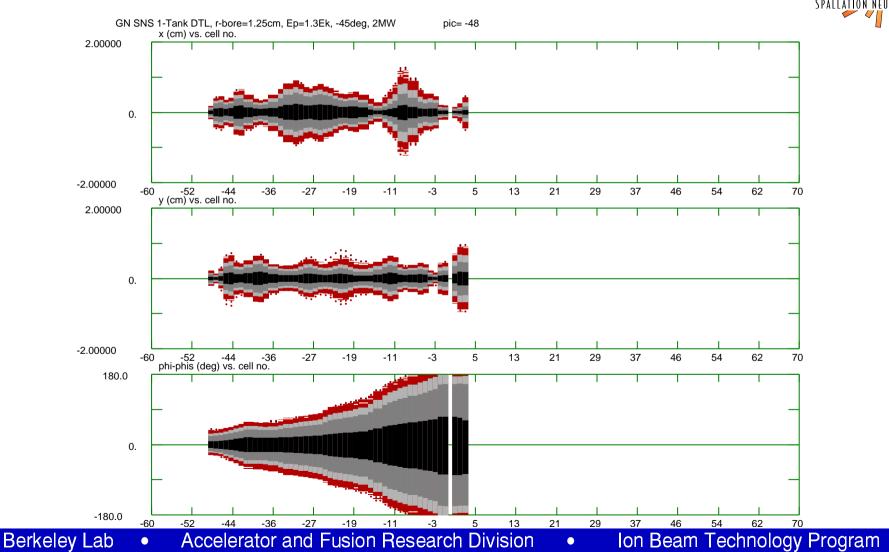
No rebunchers on





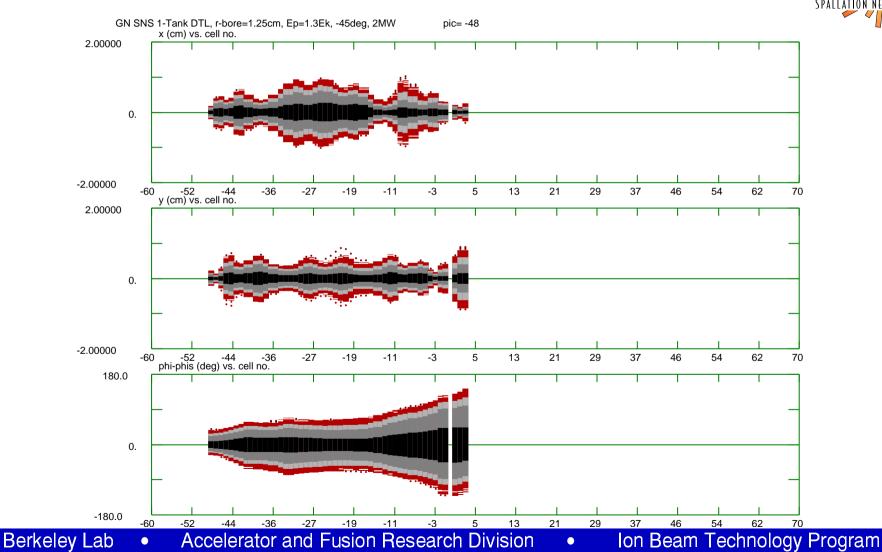
Rebuncher 1 on





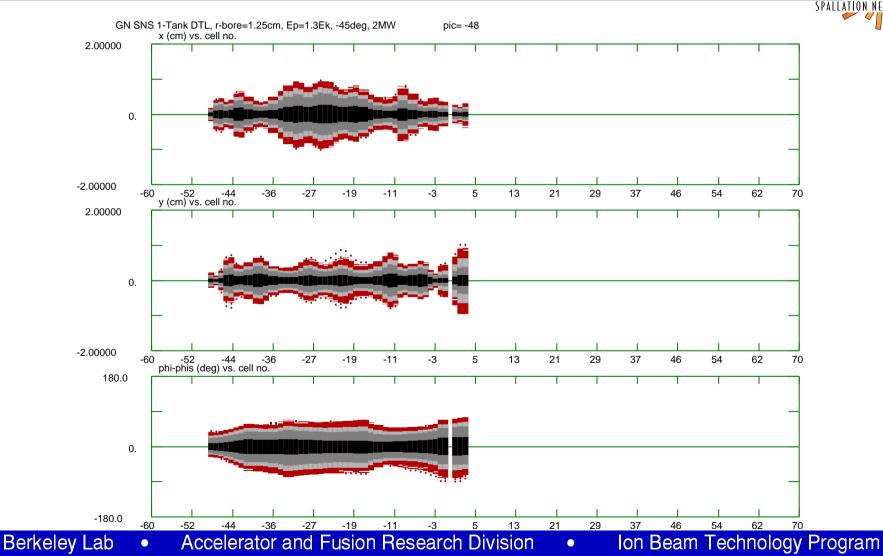
Rebunchers 1,2 on





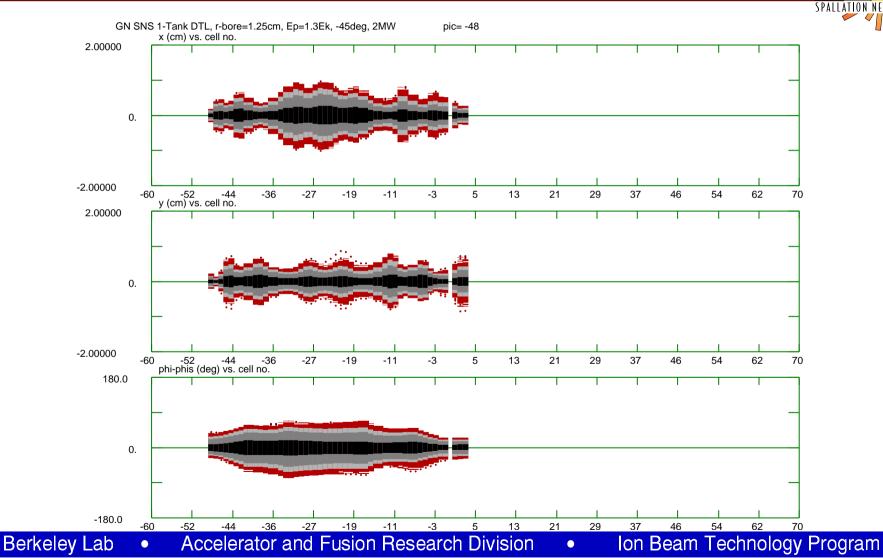
Rebunchers 1, 2, 3 on





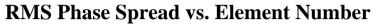
All Rebunchers on

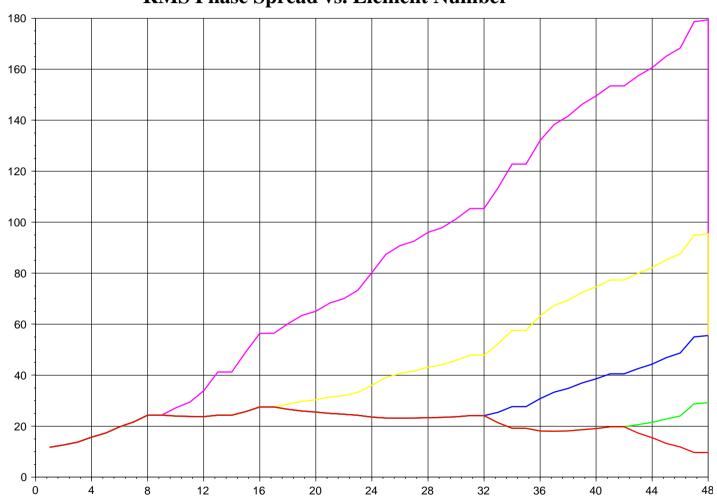




RMS Phase Spread





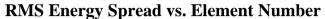


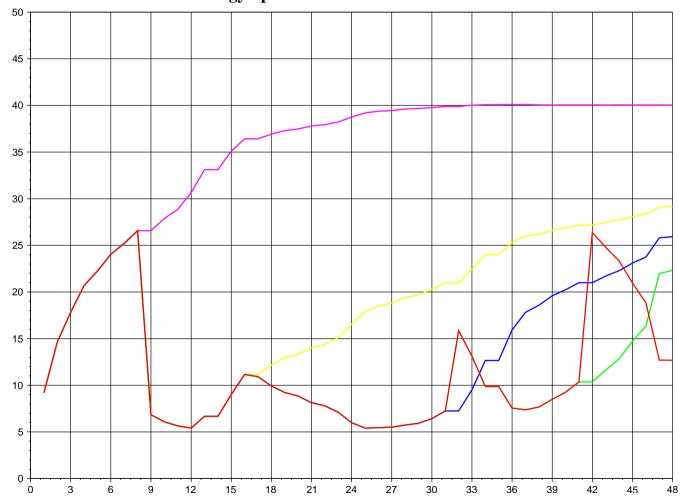
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RMS Energy Spread







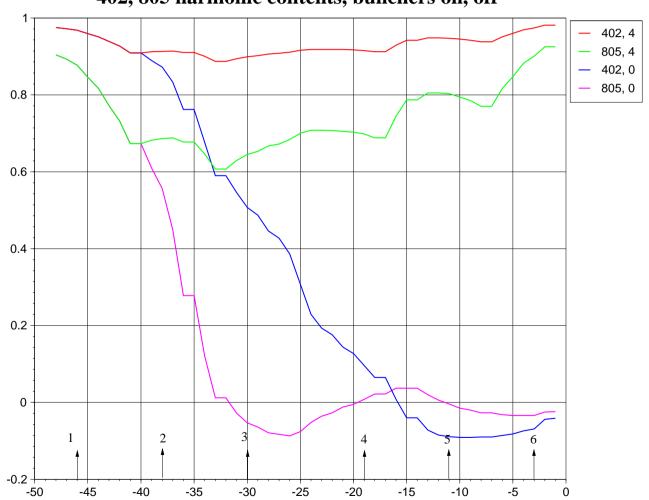
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402,805 Harmonic Content





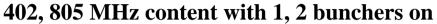


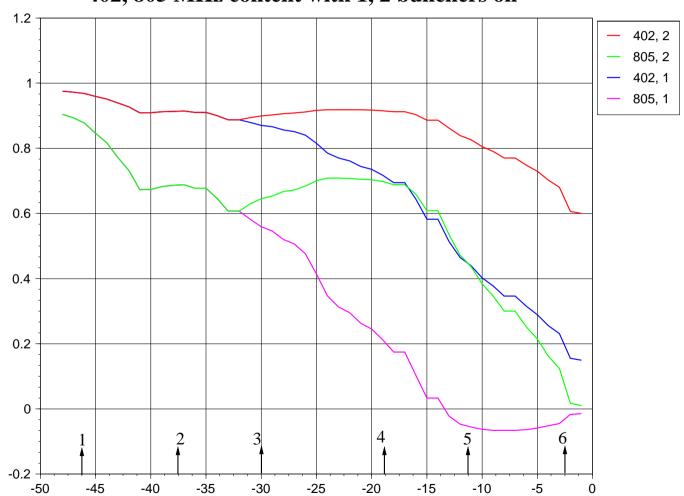
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402, 805 Harmonic Content







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Profile Monitors



- Measure x, y profile at 5 locations
- Needed to tune quads
- Non-intercepting desired
- Will use wires initially
- Power density significant
 - up to 500 kW/cm^2
 - independent of pulse length

Beam Power Density



	MEDI	「into 7.5 M	oV DTI			T			I	1		2.5	MeV
<u> </u>			-			·			;	0.070	_ energy =	2.5	! —
<u> </u>	Beam	size al broi	file monitors		<u>-</u>	<u></u>		. – – – –	beta =	0.073	_ current =	52	<u>mA</u>
Device	nc	Length	Location	alpha_x	beta_x	emitt_x	alpha_y	beta_y	emitt_y	sig(x)	sig(y) Pe	ak Pwr Densit	: у
		(cm)	(cm)		(m)	(cm-mrad)		(m)	(cm-mrad)	(cm)	(cm)	(kw/cm^2)	[
	1		0.00	-1.607	0.160	0.0203	1.983	0.196	0.0206	0.067	0.074	4173	
	2	10.45	10.45	-5.446	0.860	0.0206	-0.602	0.069	0.0205	0.156	0.044	3019	
Q1, BPM, Steer	3	6.10	16.55	2.842	1.033	0.0210	-4.324	0.321	0.0205	0.172	0.095	1265	
Scraper	4	8.40	24.95	1.805	0.634	0.0214	-10.042	1.516	0.0206	0.136	0.207	734	
Q2	. 5	6.10	31.05	-5.172	0.802	0.0215	6.145	1.793	0.0207	0.154	0.225	597	ļ
Toroid	6	8.40	39.45	-8.387	1.926	0.0217	4.107	0.922	0.0210	0.239	0.163	531	i
Q3		6.10	45.55	6.525	2.045	0.0218	-2.339	0.825	0.0211	0.247	0.154	542	i
L	8	7.95	53.50	4.642	1.153	0.0219	-3.171	1.255_	0.0212	0.186	0.191	583	: !
Reb 1	9		53.50	3.672	1.147	0.0220	-4.172	1.245	0.0214	0.186	0.191	583	
L	10	7.95	61.45	2.542	0.654	0.0221	-5. <u>6</u> 14	2.014	0.0215	0.141	0.244	604	
Q4, BPM, Steer	11	6.10	67.55	-0.274	0.527	0.0220	3.323	2.162	0.0215	0.126	0.252	651	! !
Profile	. 12	11.45	79.00	-0.741	0.645	0.0219	2.366	1.514	0.0215	0.139	0.211	705	!
Chop start	13	17.50	96.50	-1.674	1.066	0.0217	1.242	0.900_	0.0214	0.178	0.162	716	j
L	14	0.00	96.50	-1.674	1.066_	0.0217	1.242	0.899_	0.0214	0.178	0.162	716	<u> </u>
Chop end	15	17.50	114.00	-2.932	1.859	0.0218	0.455	0.616_	0.0212	0.236	0.134	657	: J
Profile	16	<u>15.50</u>	129.50	-4.259	2.925	0.0222	-0.080	0.564	0.0211	0.298	0.128	544	:
Reb 2	17	0.00	129.50	-5.782	2.918	0.0222	-0.397	0.554	0.0215	0.298	0.128	544	<u> </u>
	18	7.70	137.20	<u>-6.86</u> 2	3.838	0.0226	-0.671	0.638_	0.0214	0.345	0.137	439	! !
Q5, BPM, Steer	19	6.60	143.80	11.141	3.460	0.0229	-5.314	0.999	0.0213	0.329	0.171	368	! }
L	20	3.40	147.20	9.747	2.724	0.0231	-6.381	1.398_	0.0213	0.294	0.202	349	! :
Q6	21	6.60	153.80	1 <u>0</u> .176	2.716	0.0234	4.877	1.515	0.0213	0.295	0.210	334	<u> </u>
L	<u>i 22</u>	3.40	157.20	-11.494	3.427	0.0236	4.260	1.203	0.0213	0.333	0.187	332	<u> </u>
Q7	23	6.60	163.80	0.770	4.116	0.0241	0.299	0.921	0.0214	0.369	0.164	342	:
Chop Stop, Profile	24	13.70	177.50	0.279	3.837	0.0249	-0.071	0.890	0.0214	0.362	0.162	354	: !

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Beam Size, Continued



	25	13.70	191.20	-0.187	3.720	0.0256	-0.455	0.964	0.0213	0.361	0.168	342
Q8	26	6.60	197.80	10.382	2.956	0.0259	-4.677	1.282	0.0213	0.324	0.193	330
	27	3.40	201.20	9.009	2.285	0.0260	-5.357	1.623	0.0212	0.285	0.217	334
Q9	28	6.60	207.80	-7.419	2.188	0.0261	6.769	1.518	0.0210	0.280	0.209	354
	29	3.40	211.20	-8.374	2.720	0.0261	5.653	1.093	0.0210	0.312	0.177	374
Q10, BPM, Steer	30	6.60	217.80	5.542	2.912	0.0263	0.587	0.718	0.0211	0.324	0.144	444
	31	7.70	225.50	4.481	2.135	0.0264	0.316	0.650	0.0211	0.278	0.137	544
Reb 3	32	0.00	225.50	3.165	2.117	0.0266	-0.131	0.641	0.0213	0.278	0.137	545
	33	15.50	241.00	1.977	1.328	0.0266	-0.731	0.774	0.0213	0.220	0.150	626
Chop start	34	17.50	258.50	0.944	0.839	0.0262	-1.699	1.187	0.0213	0.174	0.186	641
L	35	0.00	258.50	0.944	0.839 !	0.0262	-1.701	1.186	0.0213	0.174	0.186	641
Chop end	36	17.50	276.00	0.178	0.664	0.0257	-3.077	1.975	0.0218	0.153	0.243	557
Profile	37	11.95	287.95	-0.265	0.682	0.0254	-4.172	2.749	0.0226	0.154	0.292	461
Q11, BPM, Steer	38	6.10	294.05	-4.800	0.965	0.0253	8.319	2.393	0.0232	0.183	0.276	410
Toroid	39	8.90	302.95	-7.341	2.040 !	0.0253	5.364	1.130	0.0239	0.266	0.192 !	405
Q12	40	6.10	309.05	7.112	2.045	0.0255	-1.894	0.933	0.0242	0.267	0.176 !	440
 	41	7.45	316.50	5.043 !	1.130 !	0.0257	-2.450	1.241 !	0.0246	0.199 !	0.204 !	508
Reb 4	42	0.00 !	316.50	3.771	1.134 !	0.0256	-3.867	1.244	0.0245	0.199 !	0.204 !	508
Ĺ	43	7.45	323.95	2.626 !	0.654	0.0257	-5.054 !	1.884	0.0249	0.152	0.254	538
Q13 !	44	6.10	330.05	-1.941	0.615	0.0258	7.609	1.676 !	0.0252	0.147 !	0.241 !	584
Emitt slit	45	8.40	338.45	-2.899	1.018	0.0258	4.439	0.658	0.0254	0.190	0.151	721
Q14, BPM, Steer	46	6.10	344.55	1.803 !	1.095	0.0258	1.075	0.351 !	0.0255	0.197 !	0.111 !	950
Profile, Emitt collector	47	19.45	364.00	0.246	0.728	0.0251	-0.496	0.249	0.0250	0.158	0.092	1417
DTL Entrance	48	1.50	365.50	1.852	0.697	0.0251	-1.280	0.275	0.0250	0.155	0.097	1378

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Power Density



- Power density typically 500 kW/cm²
- Will restrict pulse length to a few microseconds
- No tuning beam stop possible in MEBT
- MEBT chopper protection will be critical

Profile Diagnostic



- Need rapid feedback to operator
- Need ability to do multi-dimensional display of beam size vs. multiple quad tunes
- Second moment problem: some embedded software may help sort it all out

Beam Steering



- First run-thru: center in BPMs
- Check: check for quad steering
 - resolve differences
- Emittance growth reduced when steering invoked

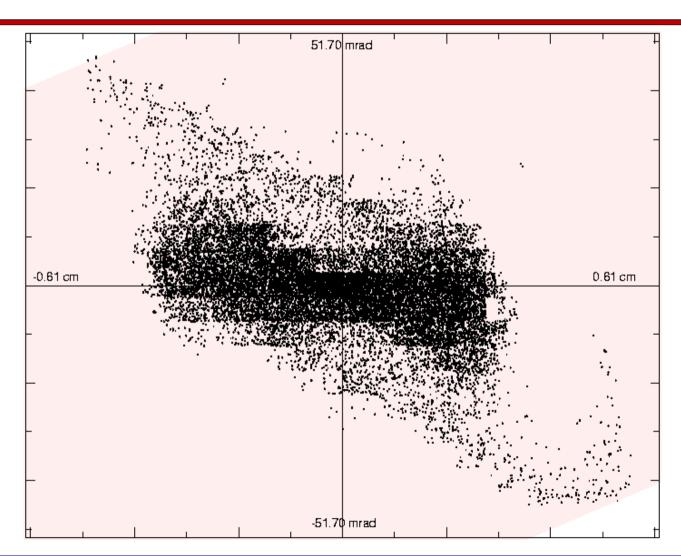
Emittance Device



- Slit, followed by collector stack
 - 50 slit positions
 - up to 64 collectors in stack
- Resolution modeled with simulator
- Power on slit must be kept very low
- Measurement in less than 10 seconds
- Short pulse, low duty factor

Sample Input Data





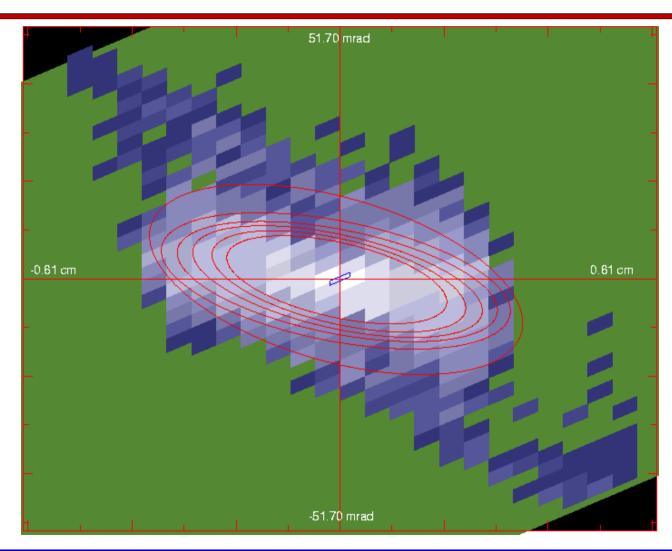
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Emittance Resolution





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Diagnostic Plate



- Temporary tuning device
- Used on RFQ and MEBT exit
- Requires 2 meter drift
- Equipment
 - fast faraday cup
 - expanded beam will debunch
 - emittance gear
 - low power only
 - 90 degree spectrometer

Warmup



- Voltage condition of
 - **LEBT**
 - **RFQ**
 - Rebuncher cavities
 - May require local 402.5 MHz clock
- Power condition plasma generator
- Beam tuning
 - with RFQ on, no convenient beam stop
 - may use LEBT chopper target

Issues Beyond FES

- Full FES commissioning will be carried out at LBNL:
 - Emittance device only at low power
 - We need sufficient time to carry this out
- At ORNL:
 - Recommission at 2.5 MeV
 - Carry beam through DTL tank 1
 - LANL tunes FES
 - What diagnostics, power limitation at 7.5 MeV?
 - Continued FES development necessary, especially on ion source

Issues 2



- Establish agreement on LANL beam acceptability and requirements for tuning and commissioning
- Identify differences between I&C HW and SW between LBNL and ORNL
- Establish trip limits for initial beam commissioning
 - protect chopper target, emittance box, etc.

Summary



- We have sufficient tools to commission FES at LBNL at full power.
- FES will provide wide range of beam parameters for downstream requirements
- Machine safety requirements must be carefully spelled out
- Continued FES development essential during installation phase of rest of accelerator components



MEBT Beam Diagnostics Review



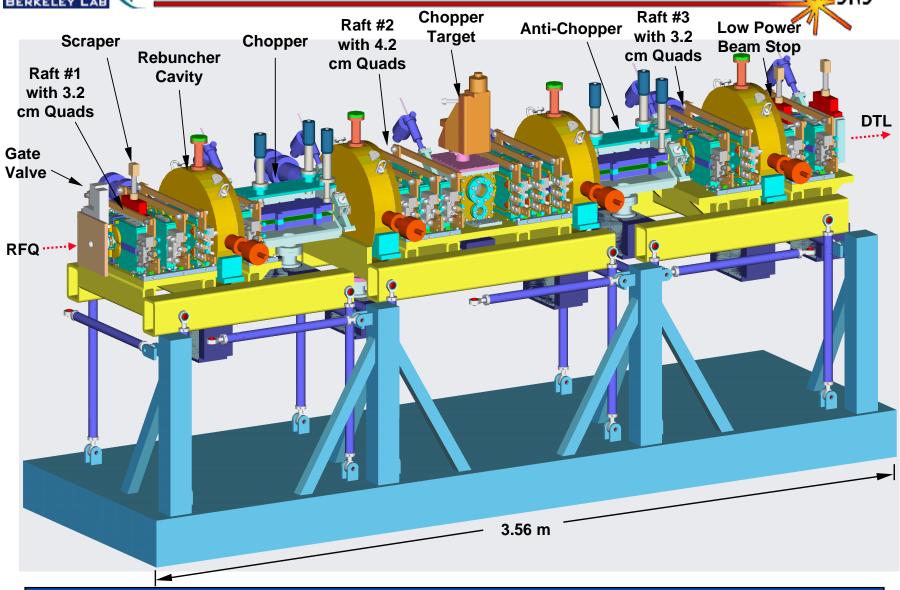
MEBT Mechanical Interfaces

Daryl Oshatz

October 12, 2000

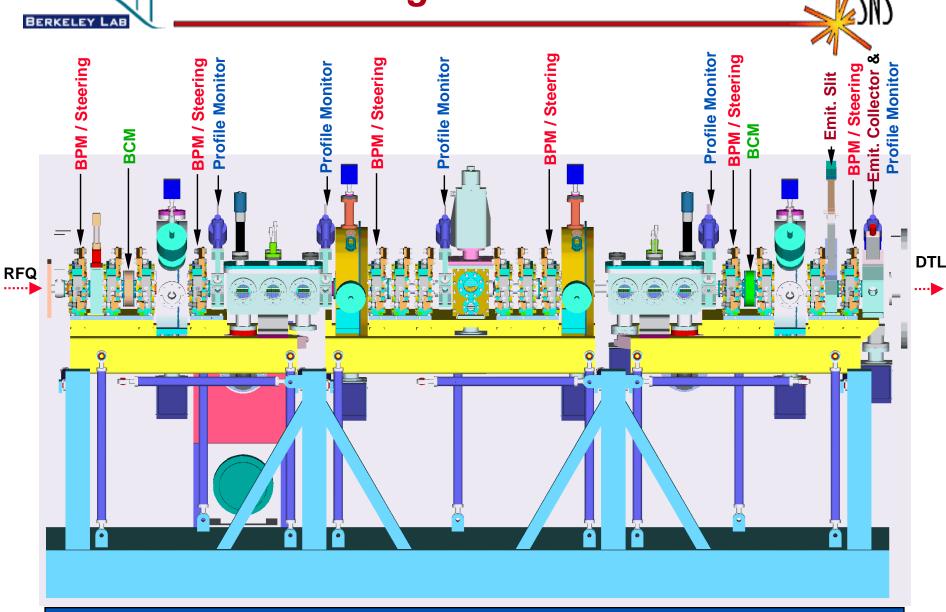


MEBT Components





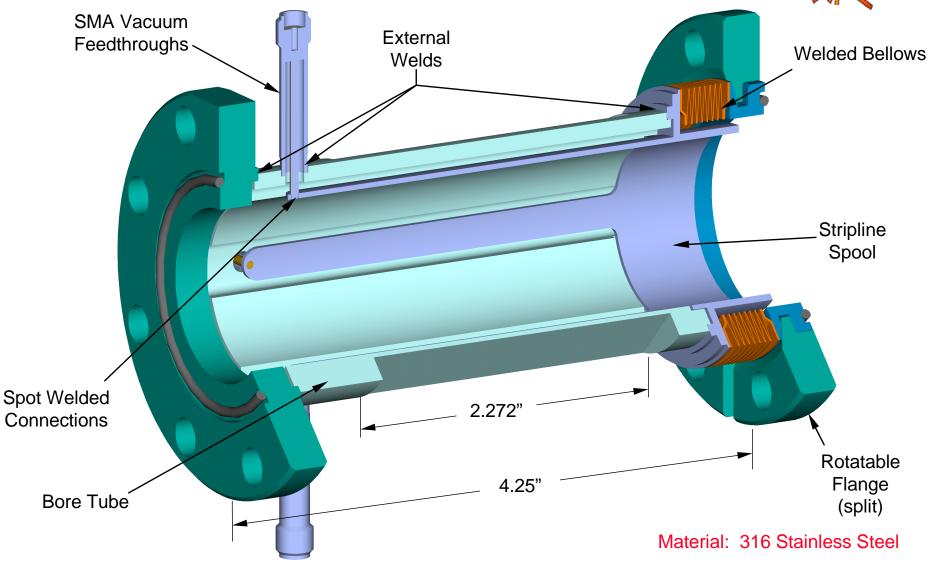
MEBT Diagnostic Locations





MEBT BPM Overview

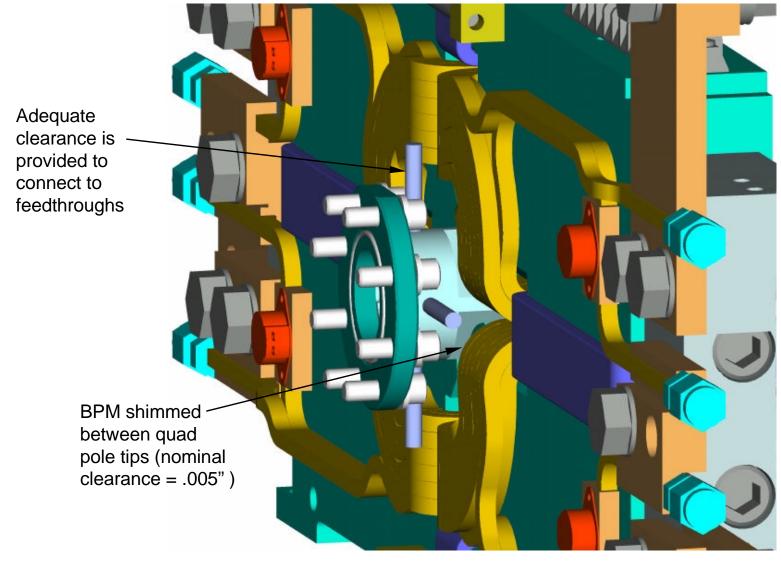






BPM Interface with Quads







BPM Fabrication Status

 Spot welding procedure has been developed and completed on all BPM's.





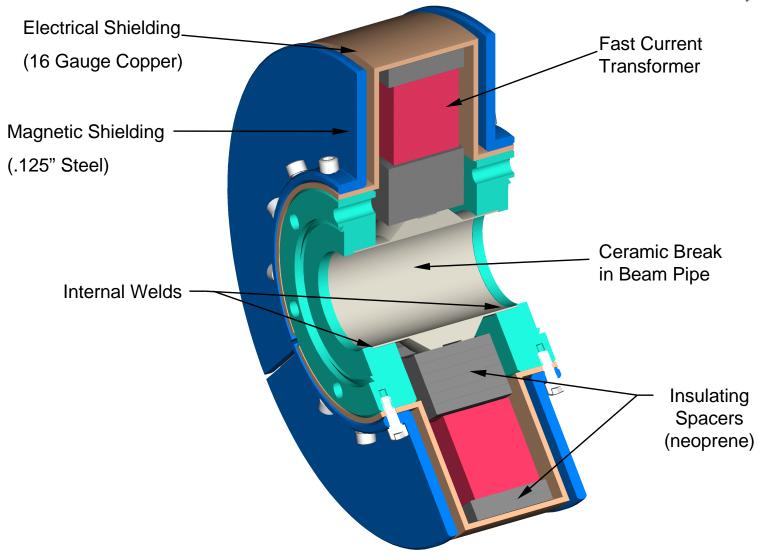
- Five of eight welded assemblies are completed.
- Some vacuum leaks have been found in SMA feedthrougs (repairable).

Related Documentation: LBNL Eng. Note M7857A, FES Technical Notes FE-EE-012, FE-ME-042



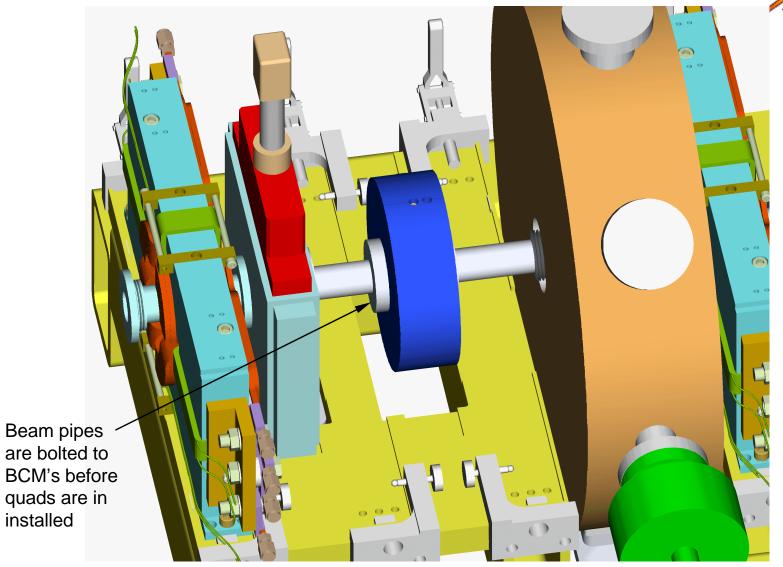
MEBT Beam Current Monitors







BCM on Raft

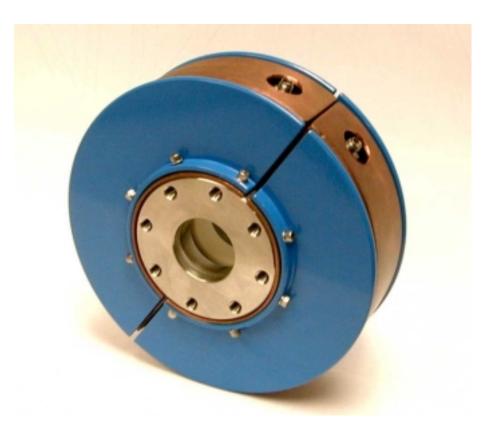




BCM Fabrication Status



- All (2) BCM assemblies are competed
- Electrical
 Measurements are complete



Related Documentation: LBNL Eng. Note M7936, FES Technical Note FE-EE-015



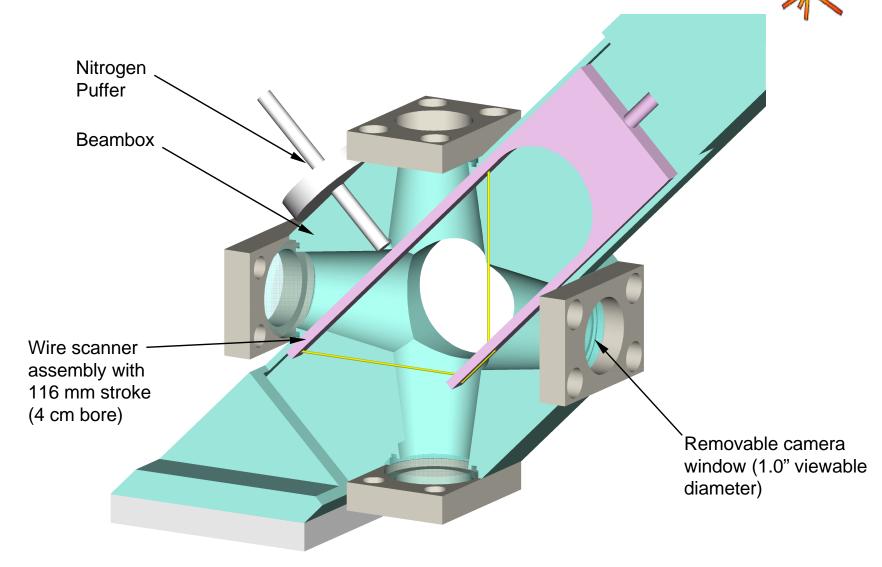
Profile Monitor / Wire Scanner



- Wire scanners will be provided in 5 locations to measure profile at low duty factor.
- Provisions will be made in the beamboxes to add on-line profile monitoring at ORNL.
- Wire scanners will be used during commissioning and for calibration of a future on-line monitoring system.



Profile Monitor Concept

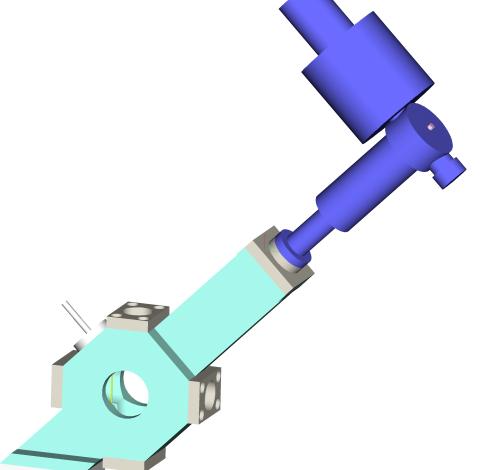




Profile Monitor Status



- Beambox at the conceptual design stage.
- Beamline interfaces are being designed to allow progress on mating components.
- BNL is working on the wire scanner assembly.

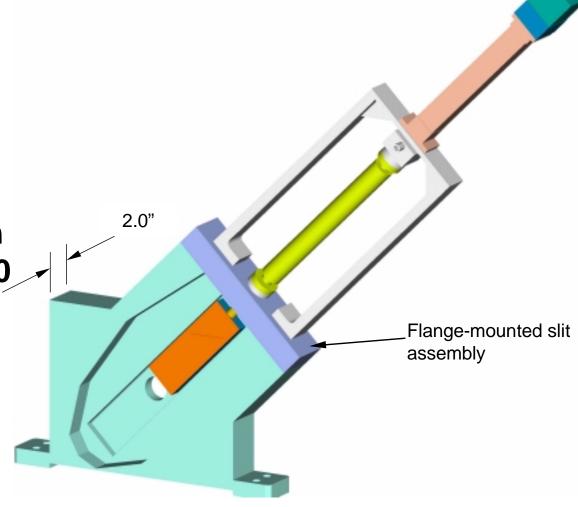




Emittance Scanner Slit

 The emittance scanner is still at the conceptual design stage.

 The main design challenge is the power density on the slits (over 600 kW/cm²).

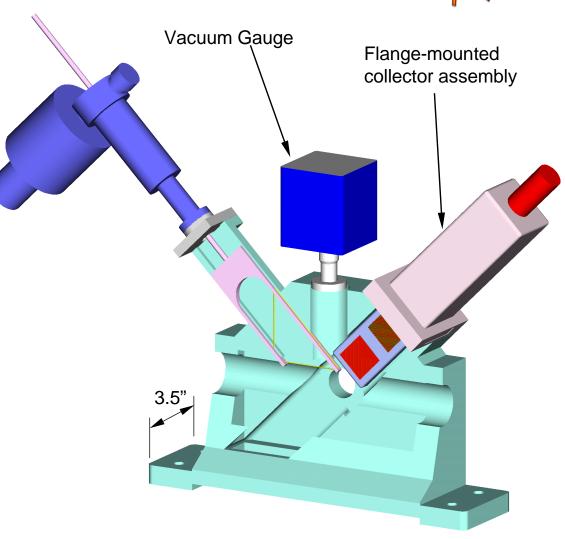




Collector /Scanner Beambox



- The emittance collector is still at the conceptual design stage.
- The emittance scanner collector shares a beambox with the last wire scanner.
- No windows are provided for optical profile measurements.





MEBT Diagnostics Review

11-12 October 2000 LBNL Steve Lewis and Tom Shea

Choice of architecture (1)



- Use direct IP for each diagnostic node with a proprietary payload:
 - Most efficient (UDP/IP)
 - Requires custom code in diagnostic node + client
 - Loses all features of IOC unless massive duplication
 - Big load on main ethernet and all subscribing OPI's
 - Gives direct access from any OPI

Choice of architecture (2)



- Each diagnostic node runs EPICS
 Portable Channel Access Server
 - Slightly less efficient (TCP/IP)
 - Easy port to any OS (already on StrongArm)
 - Minimal coding in diagnostic node ("just the drivers")
 - None in IOC: just EPICS configuration tools



- IOC can gather/process using all IOC tools (records + sequencers)
- Fixed, minimal load on main ethernet and all subscribing OPI's
- Direct access from boot servers

Primary Proposal



- Choose (2) above
- Variant (A): put on main (switched) ethernet
 - Use "obscure" PV names + access control to keep OPI's from seeing (but accessible from any OPI if required)
 - No new IOC configuration
 - Possible contention on IOC ethernet port between diagnostic traffic and rest of CA traffic



- Variant (B): put on subnet off 2nd ethernet card in each IOC
 - Requires some NRE to configure 2 ethernets/select card, etc
- Have to double-login via boot server for direct access

Secondary Proposal



- Choose (2A) above
- Migrate to (2B) only if analysis warrants and resources available

Comments



- Overall performance due to TCP/IP (embedded in CA) is highly optimized for latency/throughput tradeoff; and
- 100Mb/s switched ethernet into 200MHz+ PPC VME boards gives very good performance



- GUI in EPICS OPI level (such as Perl/Python/Matlab/...) still available
- EPICS CA includes synchronous gather with large deltaT for network skew with small deltaT for capture at each diagnostic node



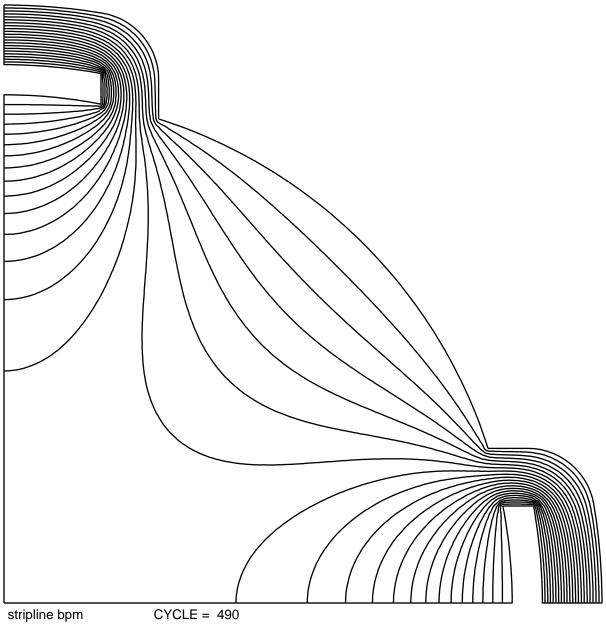
 Can still use peer-to-peer UDP/IP if needed, although correct timing design should eliminate this

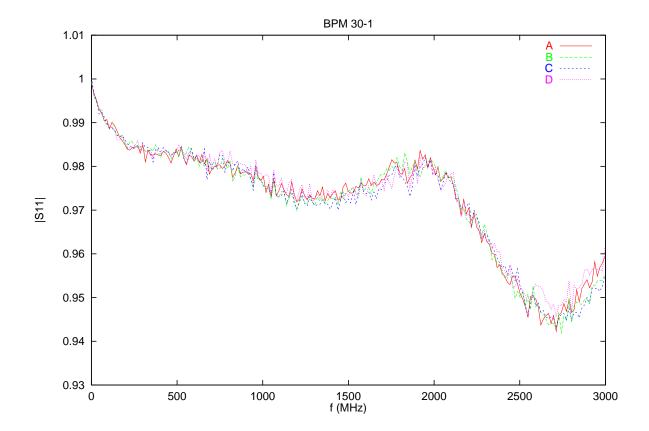
BPPM electrical design

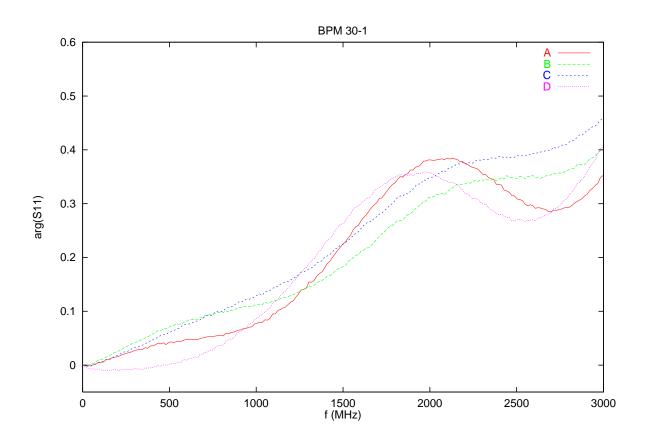
- Superfish for 50 Ohm stripline cross section, designed to fit between pole pieces of quadrupole.
- Lab measurements determine trim for L/C balance at connection to feedthrough
- Measurements of first production run
- Linearity correction: needed, but not measurable with conventional wire measurements. "Assume" Bessel function math is correct.

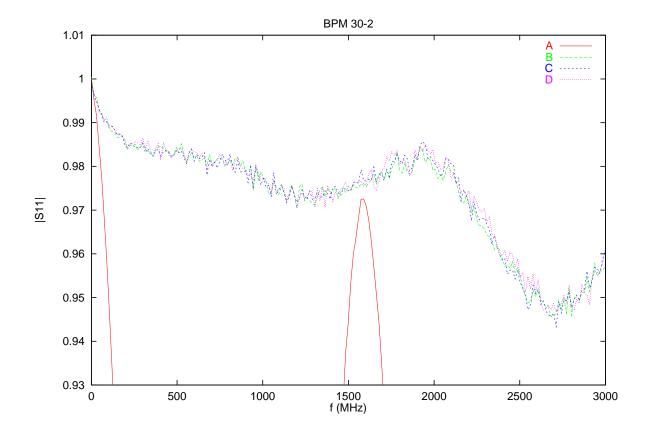
BCM electrical design

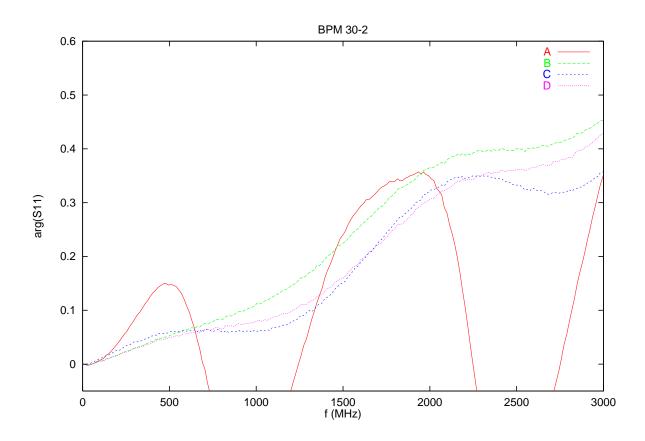
- Given target of 0.1% per microsecond droop (0.1% accuracy on approx. 1 microsecond pulses), find Bergoz device that fits MEBT space available.
- 50:1 secondary, 10 turn calibration winding
- High permeability core, proximity to Quadrupole made magnetic shielding and sensitivity a concern
- With steel shielding plate in place, measured droop next to a real Quadrupole, saw no change in droop behavior. Excitation was provided by the calibration winding.
- The FCT by itself is measured at the factory to have a risetime of 330 ps. High frequency behavior of the beamline assembly has not been measured.

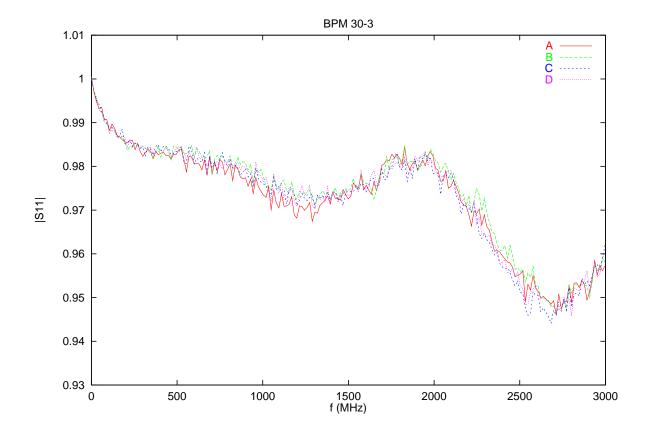


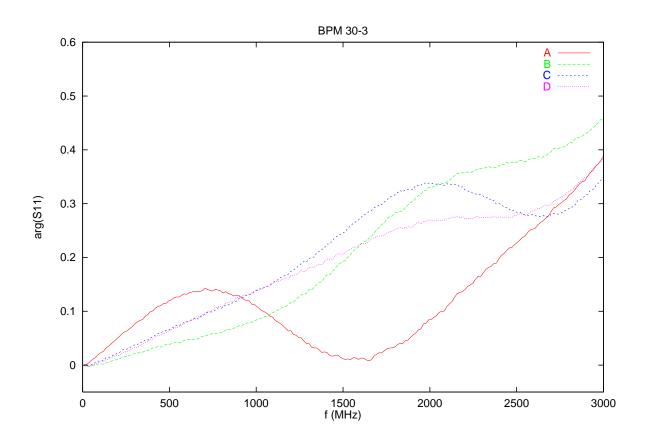


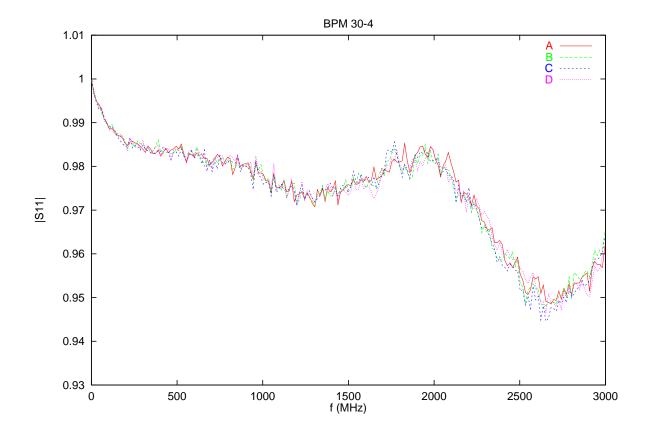


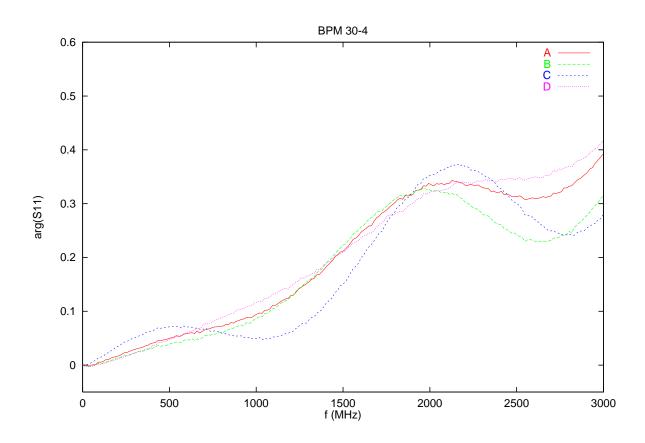


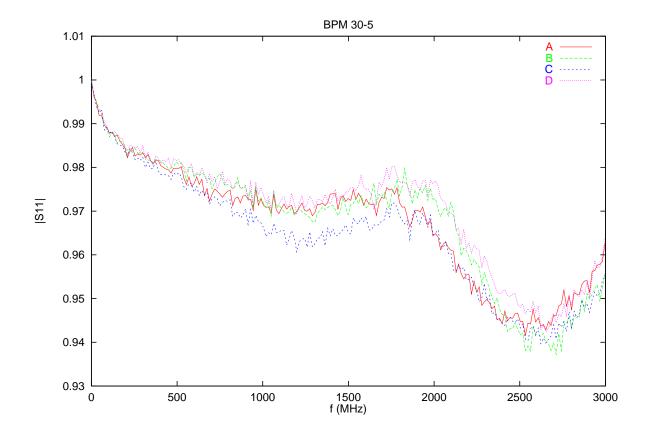


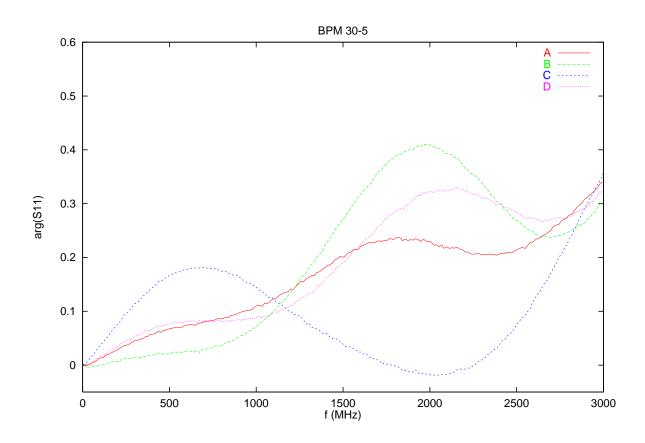


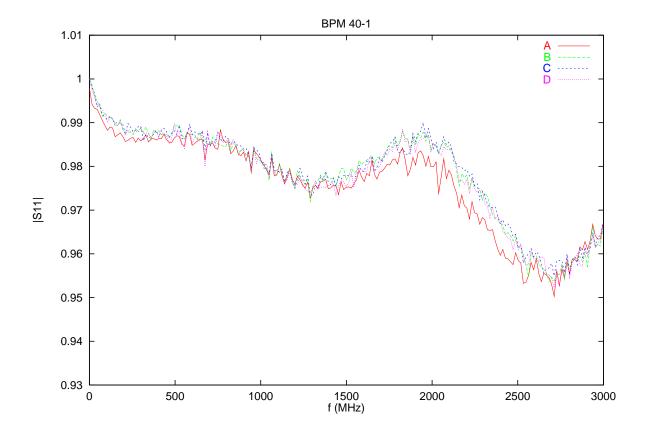


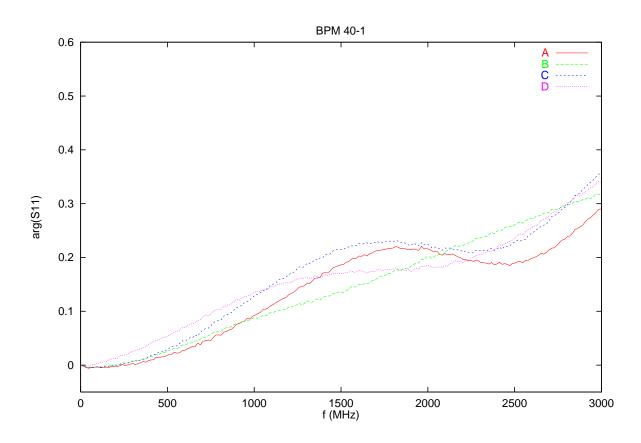


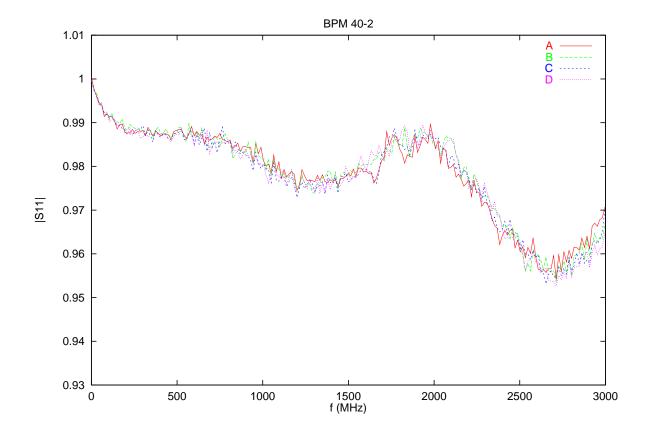


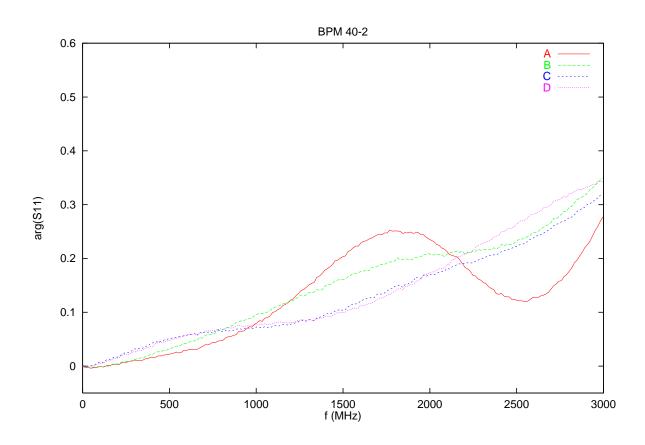


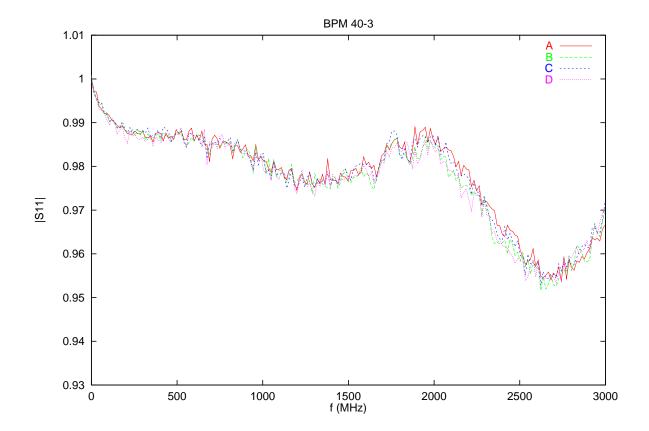


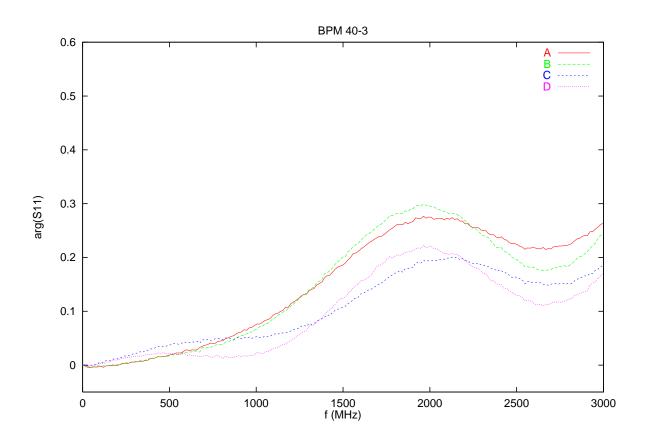


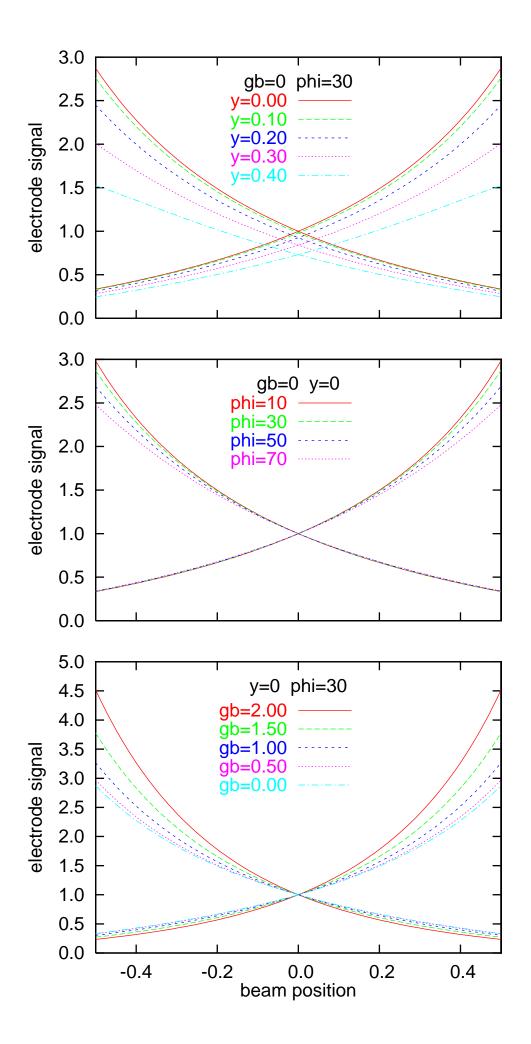


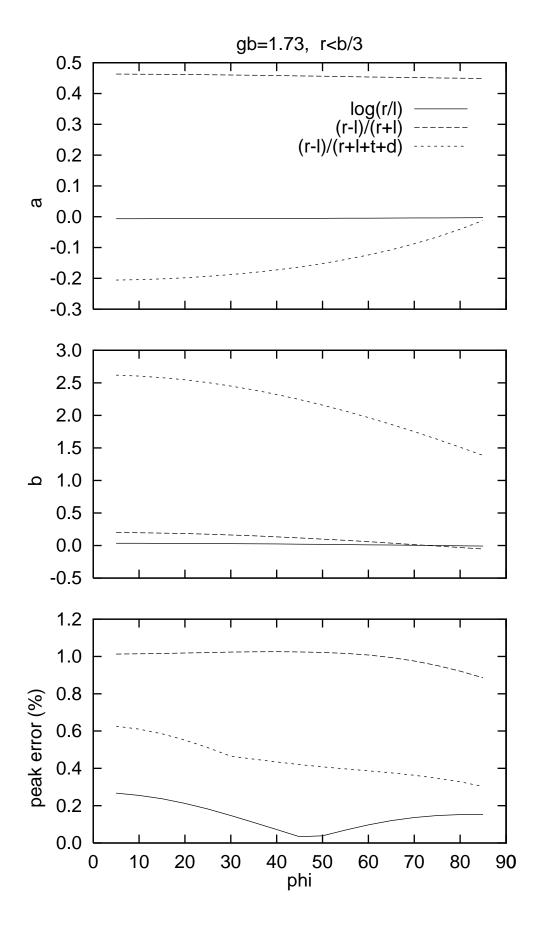


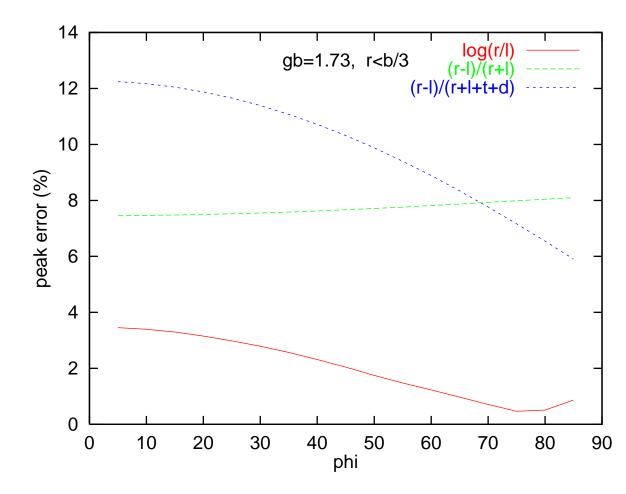














FES BPM ELECTRONICS

John Power LANL

BPM System Requirements



Measurement Frequencies 402.5/805 MHz

Measurement Bandwidth 3 MHz

Position Accuracy ± 1% of Radius

Position Resolution (Std. Dev.) 0.1% of Radius,

Phase Accuracy $\pm 2^{\circ} *$

Phase Resolution (Std. Dev.) 0.1°

Beam Current Range 14-56 mA pk

Minimum Beam Pulse Width 500 ns

^{*}For channels with a common calibration system

Linac Commissioning Minimum Requirements

Single Pulse Mode

- Any selected full-width millipulse position
- Single number
- Display update rate of 10 Hz

Multiple Pulse Mode

- Average position of N milipulses, starting M milipulses into the macropulse
- Single number
- Display update rate of 10 Hz

Array Mode

- Positions of N milipulses, starting M milipulses into the macropulse
- Array of single numbers
- Display update rate of 10 Hz

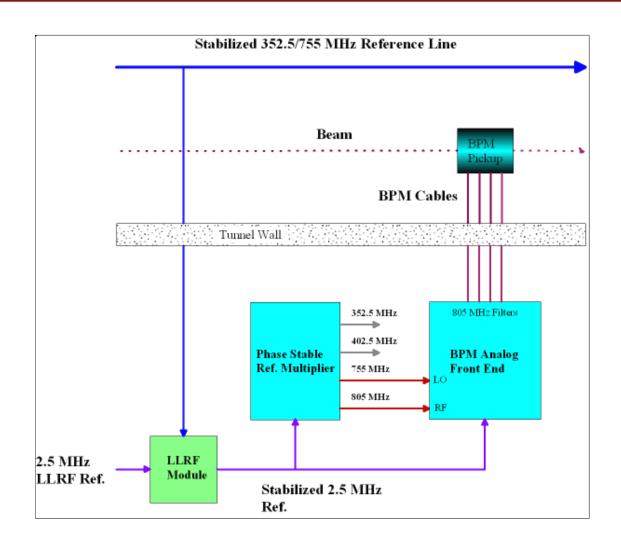
Analysis Mode

- Array of N position data points, starting M millipulses into the macropulse
- Display rate is sub-Hz (such as single shot) and may preempt normal position display operation

Other modes if needed

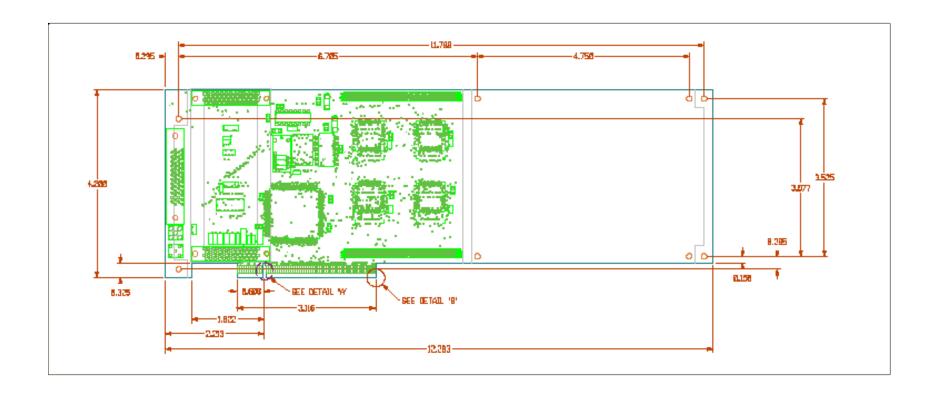
BPM Reference Signals



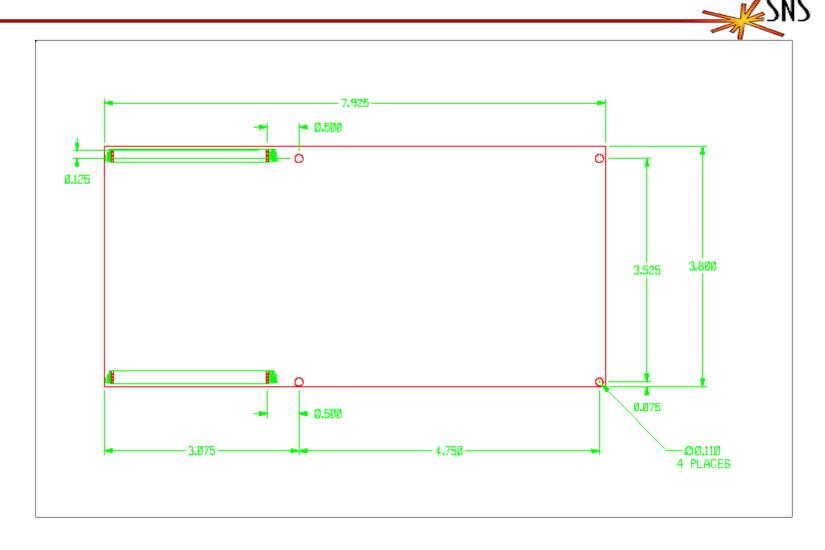


PCI Card Dimensions





Front End Daughter Card Dimensions



Electronics Specifications



Measurement Freq. 402.5/805 MHz

Intermediate Freq. 50 MHz

Local Oscillator Freq. 352.5/755 MHz

Sampling Frequency 40 MHz

Measurement Bandwidth 5 MHz

Maximum Signal Power +2 dBm

KTB @ 5 MHz BW -107 dBm

Electronics Noise Figure 17.5 dB

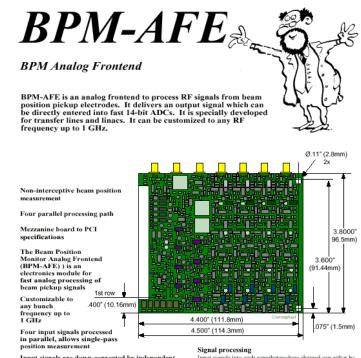
Cable Loss (100 Ft.) 3.7/5.4 dB

ADC SINAD 72 dB

SFDR 85 dB

Max. Calibration Output 6 dBm

BPM AFE Preliminary Data Sheet



Input signals are down-converted by independent superheterodyne receivers to an intermediate frequency (IF)

IF output signals are differential and galvanically isolated, for direct input into fast ADC (e.g.

Output signals are adjustable up to ±1V to take advantage of full ADC input aperture

High phase accuracy and low harmonic distortion by current feedback amplifiers IF bandwidth adjustable by separate independent

high-pass and low-pass filters provide flexibility Low power dissipation and temperature drift are

achieved with passive mixers

Excellent in-band transient response

Abuse-tolerent, by design. Hot-swap.

Signal processing linput signals into each superheterodyne channel can either be the Calibration signal or the signal from the lobe, controlled by the Lobe, Input and Calibration switches. Each channel switches are controlled individually. Calibration signals are balanced to identical level for each receiver, and can be sent to any lobe for detection by another channel, under the control of the switches. Calibration signal frequency is independent of

the superheterodyne receiver frequency. Switch-selected input signals are summed to produce a phase reference signal. Each channel is otherwise processed independently. Two successive trap filters reject unwanted harmonics. A passive double-balanced mixer processes the namionics. A passive double-benanced mixel processes the signal with a common Local foscillator (LO) signal. The common LO signal is distributed to each mixer after buffering. The resulting intermediate Frequency (IF) is filtered by two cascaded high-pass and low-pass filters to reject the unwanted mixing products.

The IF filtered signal is amplified by two stages of high gain

x bandwidth current-feedback amplifiers. The first stage can be switched between two gain levels, while the second stage gain is adjustable by potentiometer in a range 1:4.

A balun at the output produces a balanced signal with floating ground reference from each single-ended IF signal._{VD.1}

Block Diagram

Specifications

Operating frequency

Intermediate frequency

IF output bandwidth Customiz IF harmonics distortion < 50 dBc

RF input signal

IF output signal

Overall gain

Sum output

Calibration

Connectors

Power supply

Temperature drift

JFP 10/12/00

Sum phase error

Calibration switching

Calibration signal Calibration balancing

Board size:

3,800" (96,5mm) high 4,500" (114,3mm) wide

Pot adjustable in 1:4 range

+2 dBm max

±1V max

RF harmonics rejection > 60dB f2, f3 rejection Crosstalk Channel to channel: < 50 dB Calibration to channel: < 60 dB

+5V. -5V regulated

< 10-3 per degree

with 2 mounting holes per PCI specifications

Fixed range switching x1/x4 by TTL control

Customizable 60 MHz $\leq f0 \leq 1$ GHz

Customizable 10 kHz < IFBW < 1 MHz

Pot adjustable 0-4 dB above input level

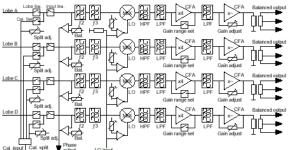
Sum balanced to 0.1 dB. On option, sum balanced to 0.01 dB

By external calibration signal < 50-ns switching, >50 dB isolation

error. On option; <0.01 dB.

+13 dBm max Splitter and switches compensated to <0.1 dB

Male HE10 60 pins (30x2) right angle header SMA jack right angle 50-ohm for RF signals (7)



Ordering information

BPM-AFE-xxxMHz BPM Frontend PCI mezzanine

On-board factory-installed options: BPM-AFE/CLM Calibration signal level matching error <0.01dB

Maintenance accessories

Table-top test kit featuring AC-DC power supply Single-ended 50-ohm output SMAs for each channel

Superheterodyne detector with 4

inputs. Resolves 0.001 dB channel-to-channel difference Phase independent! Incl. 4 Cannon pin probes Schematics and test procedures,

BPM-AFE/SCH full set with copyrights

One-time Customizing: BPM-AFE/CUS-xxxMHz

Customize BPM-AFE to xxxMHz operating frequency

Distributors

U.S.A.: GMW Associates 955 Industrial Rd.

San Carlos, CA 94070, U.S.A. Fax: (650) 802-8298 - Tel.: (650) 802-8292 sales@gmw.com

Japan: REPIC Corporation 28-3 Kita Otsuka 1-Chome

Toshima-ku, Tokyo 170-0004, Japan Fax: 03-3918-5712 - Tel.: 03-3918-5326

Manufacturer

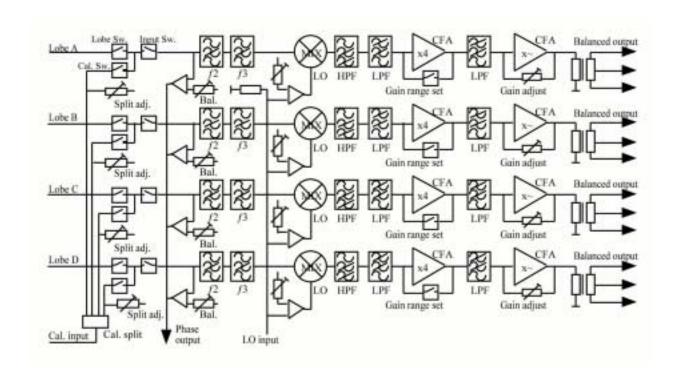
BERGOZ Instrumentation

BESCOZ: Instrumentation Espace Allondon Ouest 01630 Saint Genis Pouilly, France Fax: +33-450.426.643 - Tel.: +33-450.426.642 sales@bergoz.com

Instrumentation

AFE Preliminary Block Diagram





Diagnostics PCI data acquisition module

1.0 Overview

The Diagnostics PCI data acquisition module is designed to implement the digital portion of SNS beam diagnostic modules. Analog front end (AFE) daughter cards (which incorporate the A/D converters) plug on to the data acquisition module to complete the desired functionality. The data acquisition module provides data buffering, acquisition timing, DMA, and miscellaneous control functionality. The module's intended mode of operation is to initiate data acquisition based on a hardware timing event, buffer the data locally, and DMA the data to the host after acquisition completes. The module also supports one industry pack site in addition to the AFE daughter card, whose user pins are routed to the AFE as well as an external connector.

1.1 Capacity

The module supports 8, 16 bit data channels from the AFE. Each data channel connects to a dedicated FIFO, which is clocked by a programmable PLL clock synthesizer. The FIFO clock is common to all channels. The clock rate is selectable from 20 to 80 MHz in 10MHz steps, independent of the ADC clock.

1.2 Clocking

The module is designed to accept a 2.5MHz reference, and generate low jitter 10 and 40MHz reference clocks. These low jitter clocks are generated by a quartz stabilized PLL (TRU050) which is available in a range of output frequencies. These low jitter clocks are routed to the AFE and the digital clock synthesizer mentioned previously.

1.3 Aggregate performance

The module is designed for a maximum aggregate DMA performance of 80MB/sec when the digital section is clocked at 40MHz. This represents the maximum rate at which the FIFOs can be unloaded to host memory. Since this value is roughly 2/3 the maximum PCI bandwidth, one module can be safely used at maximum performance without compromising normal system function. The absolute maximum clock rate of the digital section will be published following the completion of functional simulations.

The maximum rate for loading the FIFOs for the AFE is 80MHz, the maximum rate allowed by the digital clock synthesizer. This corresponds to 1280MB/sec (80Mhz * 8 channels * 2 bytes/channel). Assuming 256K FIFOs, this corresponds to a maximum acquisition time of 5mS.

Obviously, data can be acquired far faster than it can be uploaded. A system design challenge will be to acquire judiciously, allowing adequate time for data transfer and processing.

2.0 Design description

The acquisition board consists of the acquisition FIFOs, an acquisition control sequencer, a DMA sequencer, a IP/Custom bus control sequencer, and a PCI master/save interface. These functional blocks are programmed by software to achieve desired operation. The sequencers are described in detail in the following sections.

2.1 Acquisition control sequencer

The acquisition control sequencer determines when the FIFOs are armed to accept data from the AFE. The sequencer may be programmed to respond to external hardware triggers and can execute

programmable delay pulse operations, where the "on" time represents a data acquisition gate. There are 64 18 bit RAM locations available for sequencer data, so multiple acquisitions based on one or more hardware events are possible. There are four external triggers available, one front panel and three for the IP site. The sequencer can set flag bits in the module status register and post interrupt requests under program control. In practice, initial firmware will be supplied with the module that performs basic acquisition functions.

2.2 DMA sequencer

The DMA control sequencer is similar to the acquisition control sequencer, only it controls the upload of data from the FIFOs to the host. The sequence and number of FIFOs to be uploaded can be programmed as desired. Obviously, the sequencer program must comply with the requirements of the PCI master interface. No hardware feature guarantees that this requirement is met. There are 64 18 bit RAM data locations available, so limited DMA chaining operations are possible. As with the acquisition sequencer, the module will be supplied with initial firmware that supports uploading all 8 FIFOs.

2.3 IP/Custom bus sequencer

The IP/Custom bus sequencer generates the Industry Pack protocol for the module's IP site, and controls several uncommitted signals and a 16 bit data buffer routed to the AFE which can be used to implement a custom bus to support programmable AFE functions. There are 64 18 bit RAM data locations available to support these operations. As with the other sequencers, no hardware feature enforces that any particular protocol is implemented. The module will be supplied with initial firmware that supports basic IP functions and a simple custom bus used on previous diagnostic designs.

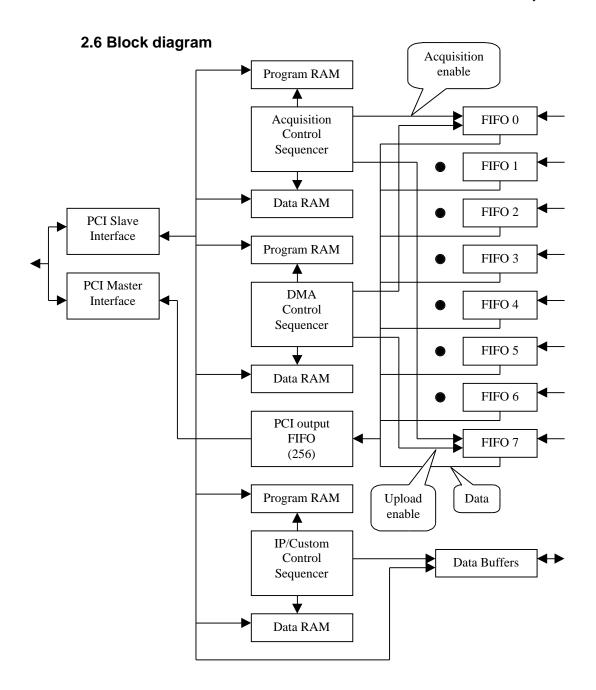
2.4 Sequencer design

All the sequencers in the module are very similar in design – the only difference being that the acquisition and DMA sequencers have 128 words of program memory, while the IP/custom bus sequencer has 64. The program words are 36 bits wide. Each sequencer contains two 8 bit counters and one 16 bit counter, supports 13 input flags and 16 output bits. A meta assembler is available to create programs. It is assumed that there will be little general interest in this level of programming, but more information will be available on the internal details as the design as simulations are completed.

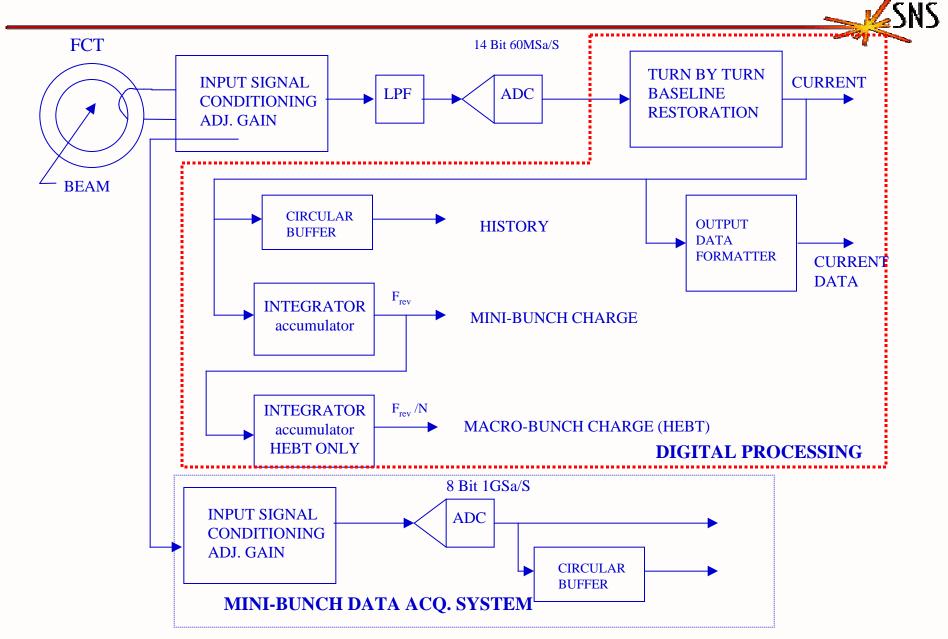
2.5 IP Module functions

The module includes a single IP site to accommodate functionality not included on the main module. The 50 user pins of the IP module are routed to the AFE and an external connector. Three of the user pins are also routed to the module's acquisition sequence's trigger inputs. The IP registers are accessible through the module's PCI address map. At this time, ID, I/O, and interrupt IP cycles are planned to be supported. IP interrupt requests set flags in the module's status register and can be enabled to generate PCI interrupts. The site is configured to the 8MHz IP standard.

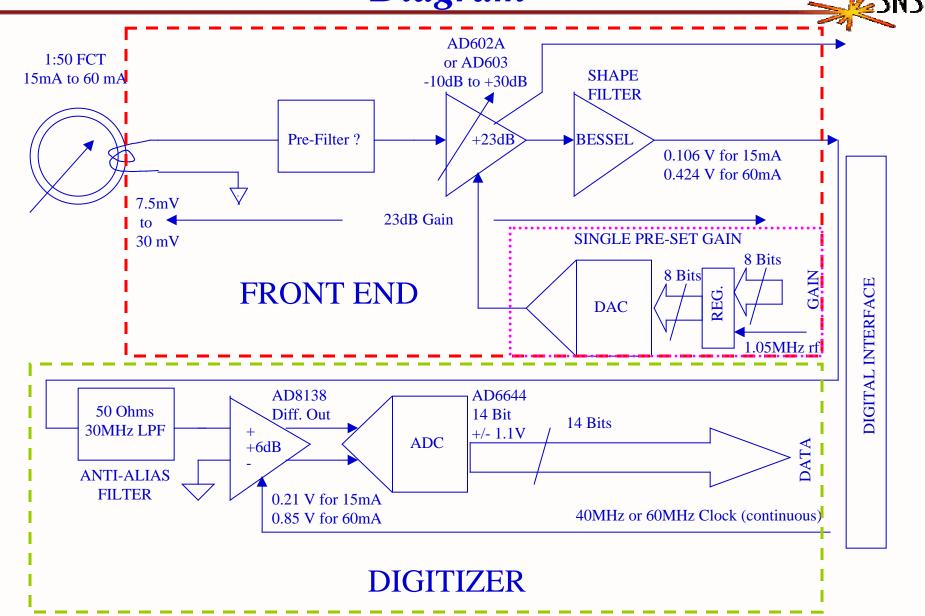
Although the IP site is intended for a standard IP module, custom protocols can be implemented by altering the firmware of the control sequencer. Choice of pins is constrained by the assignment of sequencer flags and outputs to the standard IP pinout



General BCM Signal Processing



HEBT Analog Front End & Digitizer Block Diagram

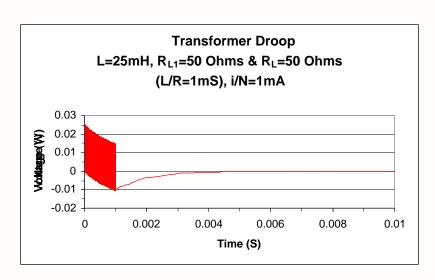


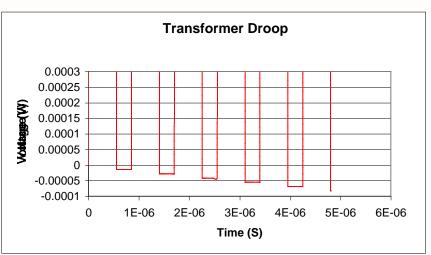
Using FCT for HEBT Averaging BCM

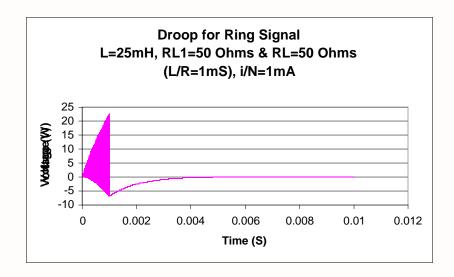
Estimated Total Input Noise for a 7MHz BW= 13uV (doubled) FCT with 1:50 Turns Ratio

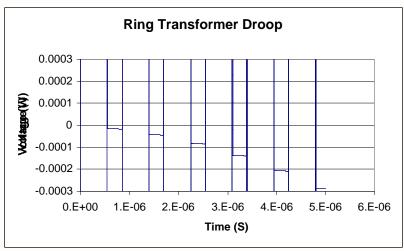
Beam Current	Est. Input Signal	Gain	Estimated Output Noise 2*G(Equiv. Input noise	Output Voltage	Resolution AD6644 Vn=133uV 14Bit ADC
15ma	7.5mV	28	of 6.5uV) 0.364mV	0.21	(1Vpk) .17%
50ma	25mV	28	0.364mV	0.7	0.05%
60ma	30mV	28	0.364mV	0.84	0.04%

Droop in Current Transformer Signals



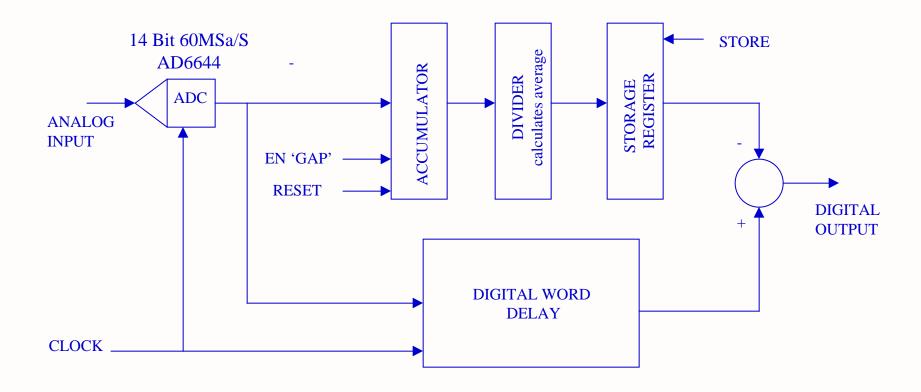






Digital Baseline Restorer





- •Accumulator enabled only during 'GAP' time
- •Baseline average stored in register & Reset each turn
- •ADC data delayed to allow time for baseline average calculation



MEBT Beam Diagnostics Review



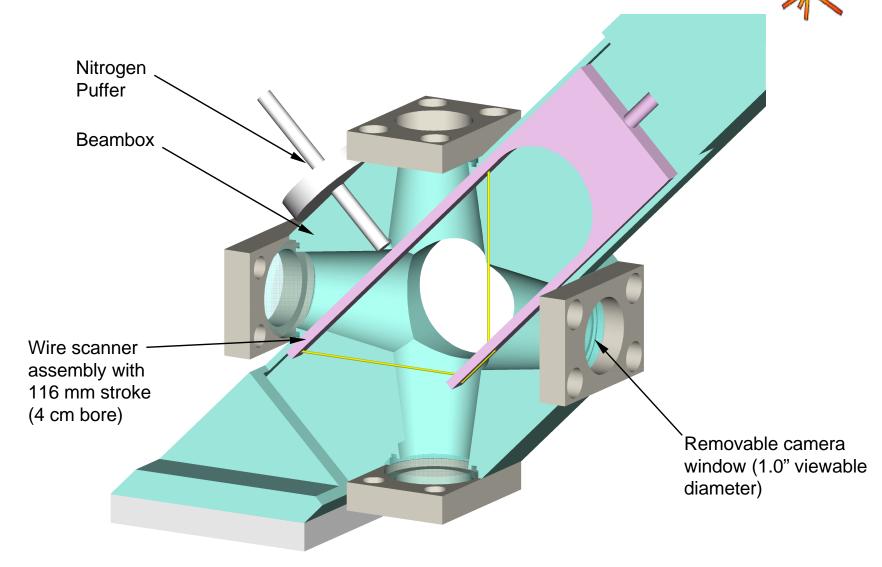
Profile Monitor Envelope and Accessibility

Daryl Oshatz

October 12, 2000



Profile Monitor Concept

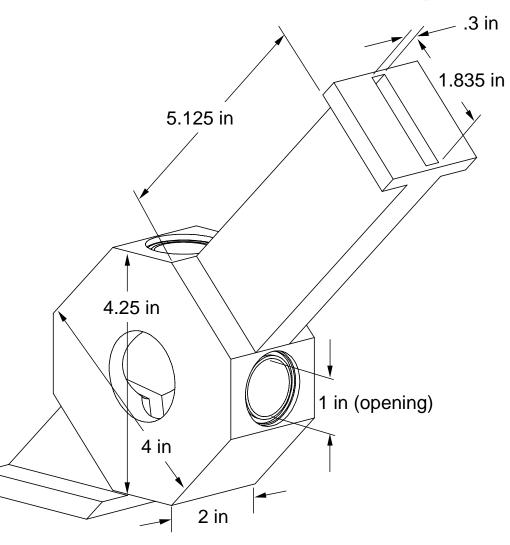




Profile Monitor Envelope

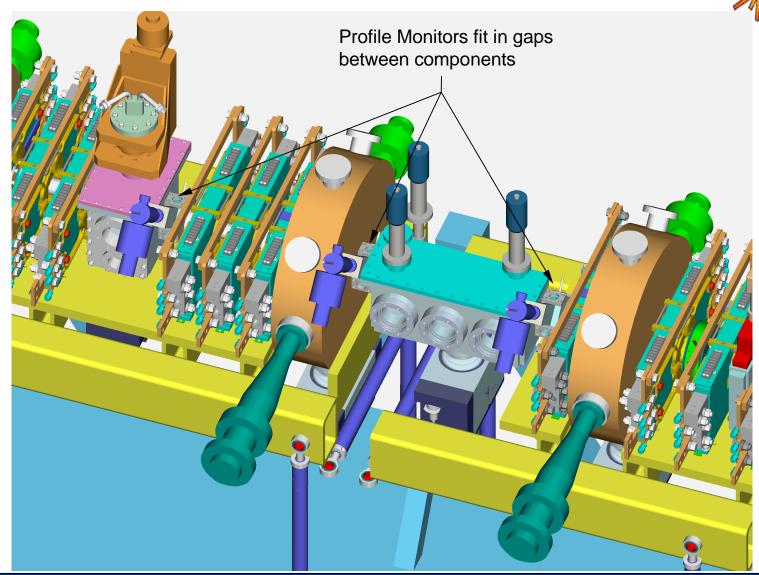


- A conceptual envelope has been defined.
- Envelope is based upon:
 - Space available between MEBT components.
 - 4 cm bore wire assembly.
 - 116 mm stroke.
 - Camera lense (f/2.8) located less than 2.8" from beam center.



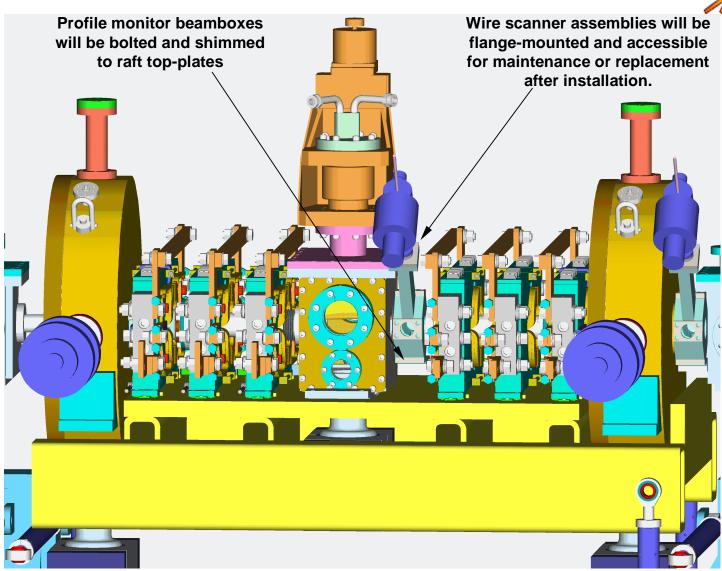


Profile Monitor Interfaces





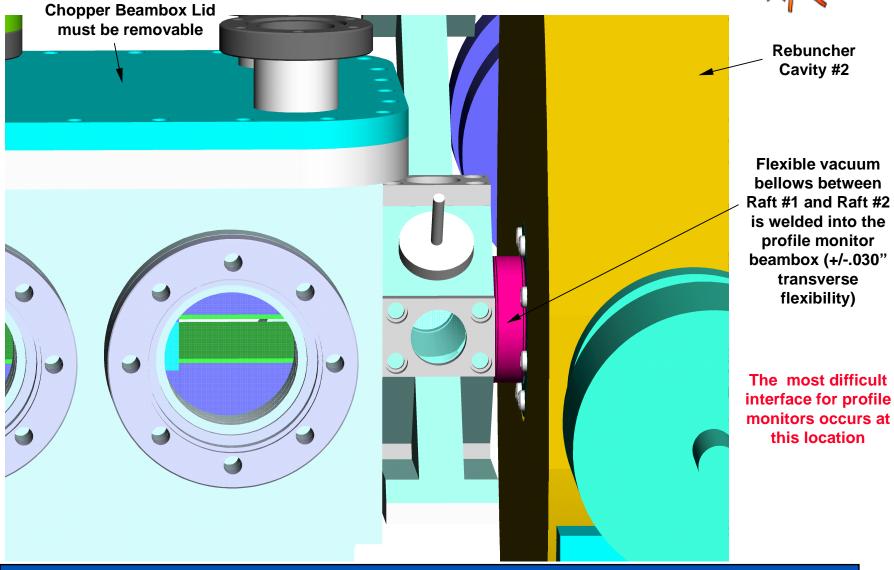
Profile Monitor Accessibility





Profile Monitor #2 Interface

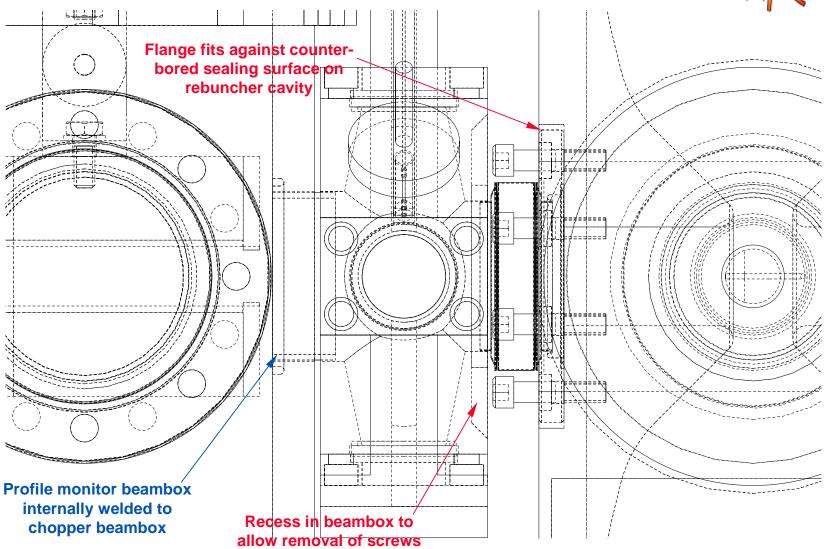






Detail of Flange Interface







SNS MEBT Carbon Wire Scanners

P. Cameron Brookhaven National Laboratory USA

SNS MEBT Wire Scanners



Contributors

- P. Cameron
- A. DellaPenna
- M. Kesselman
- C. Lac
- R. Witkover
- LANL O'Hara, Power, Stettler
- LBNL Doolittle, Oshatz

Design Requirements



- Don't melt the wire
- Sensing emission current keep temperature below 2000K
- Relative Profile Accuracy 5% at 2 ? 3 ?
- Halo Measurement 5 ?

Profile Monitors - Four Categories



- Easiest RTBT
 - Low current density, minimal wire heating
 - Large beams, positional accuracy easier
- Harder Ring
 - Higher current densities
 - Large beams, positional accuracy easier
- Hardest HEBT
 - High current densities
 - Small beams
- Impossible MEBT
 - Duty cycle

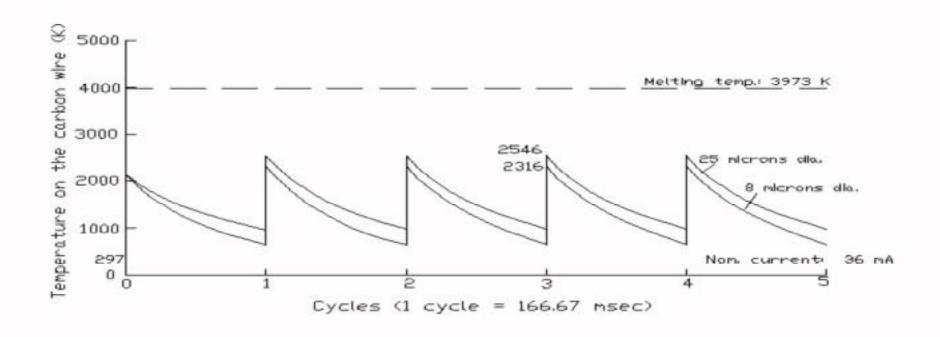
MEBT Wire Scanner Duty Cycle



- Normal machine operations
 52mA beam current during 690ns minipulse
 1000 minipulses/1ms pulse
 60 Hz pulse rate
- Diagnostics and setup machine operations
 52mA beam current during 690ns minipulse
 50-100 minipulses/50-100 µs pulse
 6 Hz pulse rate

Wire Heating - 52mA 100µs 6Hz





Velocity Criteria for Scanning and Flying Wires



Scanning - Sufficient number of Points for a good profile

```
v < 4 sigma/N period < ~ 1mm/s
sigma ~ 1 mm
N ~ 25
period ~ 167ms (6Hz)
```

• Flying slow - heating suggests to clear the beam between pulses

```
v > 4 sigma/period > 50 mm/s
sigma ~ 2 mm
```

• Flying fast - complete profile in single scan

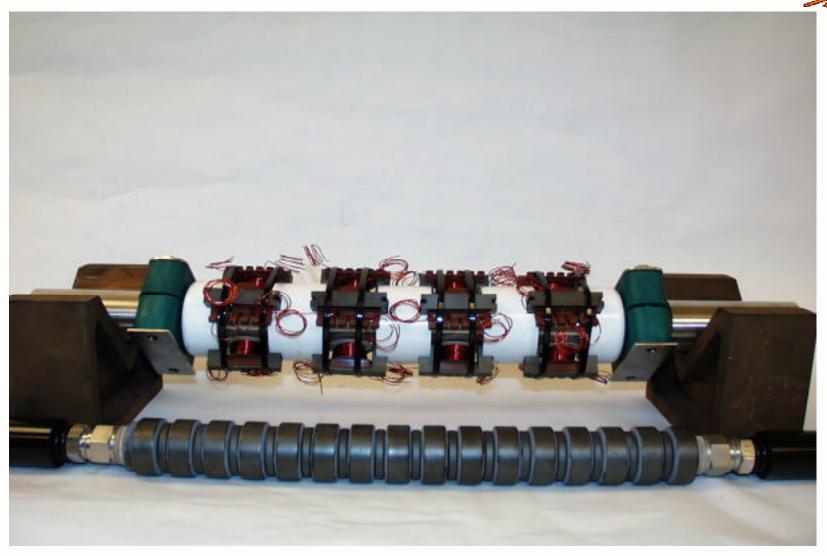
```
v > 4 sigma/period > 8 m/s
sigma ~ 2 mm
period ~ 1ms
```

Linear Stepping Motor



- Linear Stepping Motor Advantages
 - compact
 - no vacuum penetration
- Linear Stepping Motor Disadvantages
 - Vacuum linear bearings
 - Tolerances, thin wall tube fragile
 - Ferrite in vacuum especially in SRF
 - Cost?
- Velocity Limitation
 - F = ma = mv/t, or Forces varies as v squared for fixed distance
 - Practical linear velocity limit is 1 m/s > 50 mm/s
 - Single macropulse for heating

Linear Stepping Motor Prototype



Linear Motion Feedthru



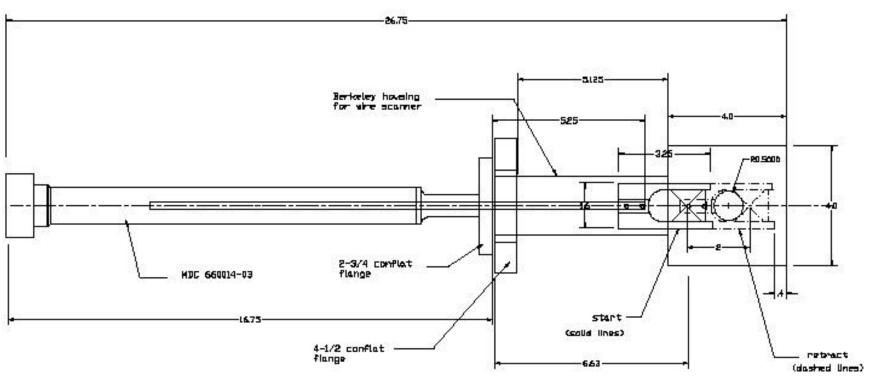
- Linear Stepping Motor Advantages
 - compact
 - cheap
- Linear Stepping Motor Disadvantages
 - Welded bellows especially in SRF
 - Formed bellows version available in shorter strokes
- Velocity Limitation
 - Manufacturer says 40 mm/s
 - < 50 mm/s for single macropulse

Linear Motion Feedthru



Linear step notor and the scanner assembly 10/8/2000 C-N-L

30 m stroke



edclinear50es1

Actuator Hardware



- Linear feedthru with stepper and encoder
 - MDC 660014-3 on 2.75CF \$1500
- Motion Control
 - National Instruments PCI-7344 \$1500
 - Compatible w/ LANL
- Analog Front End
- Digitizer
 - PCI based
- Ethernet interface

Sources of Error



Crawling wire

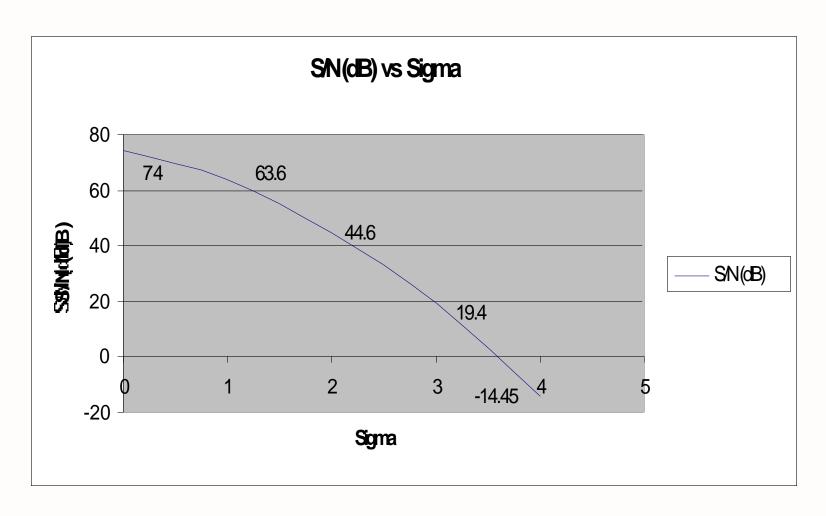
- Thermionic emission
- Drive Linearity
- Unwanted mechanical flexibility
- Beam Position jitter correlate with BPM?
- Beam Current jitter correlate with BCM?
- Errors in emission current measurement

• Flying wire (slow)

- All of the above
- Timing jitter should be negligible
- Acceleration and Velocity jitter

S/N of Emission Current Measurement





Conclusions



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- Off-the-shelf motion feedthru
- PCI motion control
- Action Items
 - Wire heating we are on the edge
 - Error budget
 - Additional mechanical support structure?
 - AFE
 - Vacuum Interface
 - Controls Interface

MEBT Diagnostics Final Design Review

Close-out Notes

Tom Shea

LBNL Berkeley, 10/12/2000

Reviewers: Tom Shea (SNS Project), Walter Barry (LBNL), Bob Shafer (LANL), Coles Sibley (SNS Project)

Comments

- 1) Mechanical design is well thought out.
- 2) Technologies being proposed are forward-looking without being excessively risky.
- 3) The deployment of MEBT diagnostics represents the first deliverable from the multi-laboratory diagnostics team. The valuable experience gained during the construction and commissioning of these systems will be applied all SNS diagnostics.
- 4) Documentation should describe the physics basis of system specifications.
- 5) As the next step in refining the controls interface, process variables and their update rates should be itemized.
- 6) It is noted that the online profile measurement is only required to resolve the profile to 3 sigma.
- 7) H- stripping in the RFQ and the attendant proton acceleration should be assessed.
- 8) Atomic electrons will provide most of the signal in the wire scanners.
- 9) Including a resistor to ground in series with the wires will allow an integrity check.
- 10) Consider adding a QA2 level current monitor for current accounting (comment from MPS review)
- 11) It would be desirable to make all presented materials available on a website.

Action Items

- 1) BNL and LBNL should agree on space allocation and beam box design. If possible the design should accommodate testing of gas fluorescence and laser wire profile monitors at LBNL or later at ORNL. (LBNL, BNL. Complete by Nov 1, 2000)
- 2) A simple integrated schedule needs to be produced. Include several milestones per system. (LBNL collects schedule input from partner labs. Complete by Nov 10, 2000)
- 3) The BPM feedthrough issue should receive a separate mini-review to assess the potential impact on MEBT reliability and, if necessary, determine a course of action. An SNS vacuum representative should review the solution. (LBNL arranges, M. Hechler reviews. Complete by Nov 17, 2000)

Summary

If the action items are completed in a timely manner, the construction of the MEBT diagnostics may proceed as presented.